Introduction

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1.1 Library Description

SEC ASIC offers STD110 as 0.25um CMOS standard cell library. SEC's 0.25um cell-based logic process providing up to 5 layers of interconnect metal with various I/O pad-pitch options such as 70um pitch pad and 80um pitch pad.

STD110 which reduced power dissipation and system cost by merging the logic and IPs as a whole and connecting internally from logic to memory data bus is ideal for high-performance products such as graphics controller, projector, portable CD and so on.

STD110 can support up to eight million gate counts of logic providing 75% of usable gate. STD110 is 25% faster than 0.35um library MDL90. Logic density is 2.3 times greater than that of MDL90. The power consumption of compiled memory is 90% smaller than MDL90.

STD110 also supports fully user-configurable compiled memory and datapath elements. Each element is provided as a compiler. Two different types of compiled memories in STD110 are available to support memories suitable to high-density and low-power applications.

To support mixed voltage environments, 2.5V, 3.3V drive and 5V-tolerant IO cells are available. LVTTL, LVCMOS, PCI, OSC, AGP, PECL, HSTL, LVDS and USB buffers are supported. To better support a system-on-chip design style, various core cells are available including processor cores like ARM7TDMI/ARM9TDMI/ ARM920T/ARM940T from ARM, Teaklite and Oak from DSPG.

The STD110 supports data transmission and communication core such as USB, IEEE1284 and UART.

The list of analog core cells includes ADC, DAC, CODEC, LVDS, RAMDAC and PLL with various bits and frequency ranges.

SEC design methodology offers an comprehensive timing driven design flow including automated time budgeting, tight floorplan synthesis intergration, powerful timing analysis and timing driven layout. Its advanced characterization flow provides accurate timing data and robust delay models for a 0.25um very deep-submicron technology. Advanced verification methods like static timing analysis and formal verification provide an effective verification methodology with a variety of simulators and cycle based simulation. SEC DFT methodology supports scan design, BIST and JTAG boundary scan. SEC provides a full set of test-ready IPs with an efficient core test integration methodology.

1.2 Features

- 2.5V standard cell library including processor and analog cores
- 0.25um five layer metal(from four layer metal option) CMOS technology
  - Logic, processor and analog
- High basic cell usages
  - Up to 8 million gates
  - Maximum usage: 75% for five layer metal
- High speed
  - Typical 2-input NAND gate delay (ND2D4): 70ps (F/O=2 + WL (0.02pF))
- Operation temperature (T_A)
  - Commercial range: 0°C to +70°C
  - Industrial range: –40°C to +85°C
- Digital cores usages
  - Hard-macro: ARM7TDMI, ARM9TDMI, ARM920T, ARM940T, Oak, Teaklite
  - Soft-macro: AMBA, DMA Controller, SDRAM Controller, Interrupt Controller, IIC, WDT, RTC, USB, IrDA, UART(16C450, 16C550), Fast Ethernet MAC, P1394a LINK, RS Decoder, Viterbi Decoder
- Analog cores usages
  - Ultra low voltage analog core (2.5V and 1.8V) available
  - Analog core supply voltage:
    2.5V analog core: 2.5V ± 5%
    1.8V analog core: 1.8V ± 5%
  - ADC: 8bit (30M, 2.5V), 10bit ((30M, 100M, 2.5V), (250K, 20M, 1.8V)), 12bit (200K, 20M, 2.5V)
  - DAC: 8bit (2M, 2.5V), 10bit ((300M, 2.5V), (2M, 1.8V)), 12bit ((2M, 2.5V), (80M, 1.8V))
  - CODEC: 8bit (8K~11K), 16bit (44.1K)
  - PLL: 25M ~ 300M (FSPLL, 2.5V), 1G (PLL, 1.8V), 20M ~ 170M(FSPLL, 1.8V)
  - Others: 300M (RAMDAC+PLL)
- Fully user-configurable Static RAMs and ROMs
  - High-density and low-power memory available
  - Duty-free cycle in synchronous memory available
  - 2-bank architecture available
  - Flexible aspect ratio available
  - Up to 256K-bit single-port SRAM available.
  - Up to 128K-bit dual-port SRAM available.
  - Up to 512K-bit diffusion and metal-2 ROM available.
  - Up to 16K-bit multi-port register file available.
  - Up to 32K-bit FIFO available.
- Fully configurable datapath macrocells
  - 4 ~ 64 bit adder available
  - 4 ~ 64 bit barrel shifter available
  - 6 ~ 64 bit multiplier with 1-stage pipeline available
  - Various output driver strength available
  - A tightly integrate apollo, Avant!, design environment
- I/O cells
  - 2.5V/3.3V and 5V tolerant IO
  - 3-level (high, medium, no) slew rate control
  - 1/2/4/6/8/10/12mA available for 3.3V and 2.5V output buffers
  - 1/2/3mA available for 5V-tolerant output buffers

- IO IP available
  - PCI ((33MHz, 66MHz, 3.3V), (33MHz, 3.3/5V tolerant))
  - USB (full speed/low speed)
  - SSTL2 (DDR SDRAM interface, up to 200MHz)
  - AGP (AGP2.0 Compliant, 66MHz@1X,133MHz@2X, 266MHz@4X)
  - PECL (2.5V interface, up to 400MHz)
  - HSTL (class1, class2, 30MHz)
  - LVDS (3.3V(2.5V optional) interface, 300MHz)
- Various package options
  - QFP, thin QFP, power QFP, plastic BGA, super BGA, plastic leaded chip carrier, etc.
- Fully integrated CAD software and EDA support
  - Logic synthesis: Synopsys Design Compiler
  - Logic simulation: Cadence Verilog-XL, Cadence NC-Verilog, Viewlogic ViewSim, Mentor ModelSim-VHDL, Mentor ModelSim-Verilog, Synopsys VSS, Synopsys VCS
  - Scan insertion and ATPG: Synopsys TestGen, Synopsys Test Compiler, Mentor Fastscan
  - Static timing analysis: Synopsys PrimeTime, Synopsys MOTIVE
  - RC analysis: Avant! Star-RC
  - Power analysis: Synopsys DesignPower, CubicPower (In-House Tool)
  - Formal verification: Synopsys Formality, Chrysalis Design VERIFYer, Verplex Tuxedo-LEC
  - Fault simulation: Cadence Verifault, SuperTest (In-House Tool)
  - Delay calculator: CubicDelay (In-House Tool)

- STD110 contains 12 user selectable clock tree cells(CTC). At the pre-layout design stage, these will be used as the cells which represent actual clock tree informatin of P&R. The key features of new SEC ASIC CTS flow are as follows:
  - 12 user selectable clock tree cells(CTC) for STD110
  - Good pre-layout and post-layout correlation
  - No customer netlist modification
  - Accurate post-layout back-annotation mechanism
  - Insertion delay, skew, transition time management
  - Clock tree information file generation
  - Cover 100 to 30,000 fanouts and up to 1M gate count for CTS spanning block (GCCSB)
  - Tightly coupled with SEC in-house delay calculator, CubicDelay Gated CTS support
  - Hierarchical/Flatten verilog, edif interface for P&R

For more detail information for CTC flow, refer to “CTC flow guideline for CubicDelay” included in SEC ASIC design kit.

1.3 EDA Support

SEC ASIC provides an efficient solution for multi-million gate ASICs in very deep submicron (VDSM) technology. For large system-on-chip (SOC) type designs, static verification methodology (static timing analysis and formal verification) will shorten your design cycle time, which in turn will lessen today's ever-increasing time-to-market pressure. Our Design-for-Test (DFT) methodology and service take you through all phases of test insertion, test pattern generation and fault grading to get high test coverage.

STD110 supports a rich collection of industry-standard EDA tools from Cadence, Synopsys, Mentor graphics, and Avant! on multiple design platforms such as Solaris and HP. Customers are allowed to choose among the industry-leading EDA tools from design capture, synthesis, simulation, and DFT to layout. Several powerful proprietary software tools are seamlessly integrated in our design kits to improve your product quality.

For high simulation accuracy, STD110 uses a proprietary delay calculator. Cell delay is calculated based on a matrix of delay parameters for each macrocell, and signal interconnect delay is calculated based on the RC tree analysis.

1.4 Product Family

STD110 library include the following design elements:

- Analog core cells
- Digital core cells
- Internal macrocells
- Compiled macrocells
- Input/Output cells.

1.4.1 ANALOG CORE CELLS

Introduction to Analog Cores

SEC ASIC is one of the leading suppliers of cell based mixed analog and digital designs. As a leading supplier of mixed analog and digital designs, SEC ASIC has more analog design experience than any other vendors. Analog has been and will continue to be a part of the strategic focus at SEC ASIC. Analog design is a part of the total SEC ASIC integrated design system. Workstation symbols are supplied for analog cells and are entered as part of the design by the customer or design center. SEC ASIC uses basically the same automatic layout and verification tools for analog cells as for digital cells. Analog designs are processed on the same production line as digital designs.

SEC's analog core family comprises ADC,DAC,PLL and sigma-delta ADC/DAC, and their brief functional descriptions are introduced below.
[data sheets for all analog cores available]

Analog-to-Digital Converters

Analog-to-digital converters provide the link between the analog world and digital systems. Due to their extensive use of analog and mixed analog-digital operations, A/D converters often appear as the bottleneck in data processing applications, limiting the overall speed or precision.

An A/D converter produces a digital output, D, as a function of the analog input, A:

$$D = f(A)$$

While the input can assume an infinite number of values, the output can be selected from only a finite set of codes given by the converter's output word length(i.e, resolution). Thus, the ADC must approximate each input level with one of these codes, this process is so called 'quantization'.

In a digital system the amplitude is quantized into discrete steps, and at the same time the signal is sampled at discrete time intervals. This time interval is called sampling time or sampling frequency. After sampling and quantization process, the analog signal(A) becomes digital output (D).

Digital-to-Analog Converters

The D/A converters are the digital-to-analog conversion circuits, which are also called DACs. They can be considered as decoding devices that accept digitally coded signals and provide analog output in the form of currents or voltages. In this manner, they provide an interface between the digital signal of the computer systems and continuous signals of analog world. They are employed in a variety of applications, from CRT display systems and voice sythesizers to automatic test systems, digital controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters.

Figure 1 shows the functional block diagram of a basic D/A converter system. The input to the D/A converter is a digital word, made up a stream of binary bits comprised of 1's and 0's. The output analog quantity A, which can be a voltage or current, is related to the input as

$$A = KV_{REF}\left[\frac{b1}{2^1}+\frac{b2}{2^2}+\ldots+\frac{bn}{2^n}\right]$$

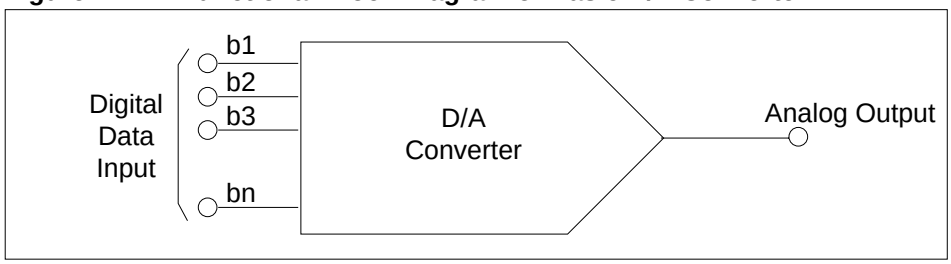
where K is a scale factor, V_{REF} is a reference voltage, n is the total number of bits, and b1,b2,...,bn are the bit coefficients, which are quntized to be a 1 or a 0.

As a function of the input binary word which determines the bit coefficients, the output exhibits 2^n discrete voltage level ranging from zero to a maximum value of

$$Vo(max) = V_{REF}\frac{2^n-1}{2^n}$$

with a minimum step change ΔVo given as $\Delta Vo = \frac{V_{REF}}{2^n}$ \

Figure 1-1. Functional Block Diagram of Basic D/A Converter



Sigma-Delta ADC/DAC

VLSI offers high speed and high density, but reduced accuracy for analog components and reduced signal range (reduced dynamic range). Hence, an exchange of digital complexity and of resolution in time for resolution in signal amplitude is needed. So good solution is over-sampling data converter. Oversampling sigma-delta converter is used in slow speed (audio band) application because of process limit. It's noise shaping (sigma-delta) feature make high resolution about max. SND=90~100dB

In ADC path, analog single input is converted to differential signal with anti-aliasing filtering through anti-aliasing filter block. And sigma-delta modulator converts the signal into oversampled noise-shaping 1bit PDM (Pulse Density Modulation). Following digital decimation filter reject the out of band noise and outputs 16bits high resolution digital data with down sampled to Fs rate. In DAC path, digital input data is oversampled by interpolation filter and it is converted to noise-shaped 1bit PDM through digital sigma-delta modulator. Analog SC-post-filter rejects the out of band noise. And anti-image filter rejects sampling images and outputs single analog signal with high resolution.

Phase Locked Loop

Samsung's PLL cores implemented as an analog function provide frequency multiplication capabilities and enable system designers to synchronize ASIC chip-level clock networks with a common reference signal.

In the past, designers wishing to incorporate a PLL into a digital design environment had only two options:

(1) A special mixed-signal process to incorporate analog functions onto the chip
(2) An all digital PLL that can be incorporated into a standard digital process.

However, a mixed-signal process is too expensive to be a feasible solution. On the other hand digital PLLs typically require huge silicon area and exhibits poor locking time despite their high accuracy.

Differing from the previous solutions, Samsung's PLL cores can be implemented on standard digital CMOS process while functioning as an analog PLL.

Samsung's PLL cores:
* Require only a few off-chip passive components for the whole function
* Remove the need for an expensive mixed-signal process
* Provide faster locking time than all digital PLLs
* Present low jitter characteristics

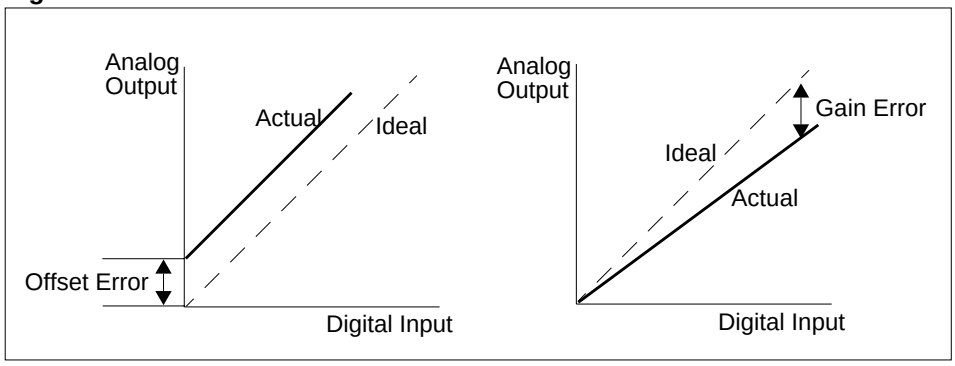
Glossary by Core Families

1. Digital-to-Analog Converter

1. Resolution - An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have resolution of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span.

2. Accuracy - Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Source of error include gain error, offset error, linearity errors and noise. Error is usually commensurate with resolution, less than $2^{-(n+1)}$, or 1/2 LSB of full scale.

Figure 1-2. Error of D/A Converter



3. LSB (Least-Significant Bit) - In a system in which a numerical magnitude is represented by a series of binary digits, the LSB is that bit that carries the smallest value or weight. It represents the smallest analog change that can be resolved by an n-bit converter.

$$\text{LSB (Analog Value)} = \text{FSR}/2^n$$

FSR = Full-Scale Range, n = number of bits

4. MSB (Most-Significant Bit) - The binary digit with the largest numerical weighting. Normally, the MSB of a digital word has a weighting of 1/2 the full range.

5. Compliance-Voltage Range - For a current output DAC, the maximum range of(output) terminal voltage for which the device will provide the specified current-output characteristics.

6. Glitch - A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage (V*ns) or current (mA*ns) and time duration or charge transferred.

7. Harmonic Distortion (and Total Harmonic Distortion) - The DAC is driven by the digitized representation of sine wave. The ratio of the RMS sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second through fifth.

$$\text{THD} = 20\log\frac{(V2^2 + V3^2 + V4^2 + V5^2)^{1/2}}{V1}$$

V1: RMS amplitude of the fundamental

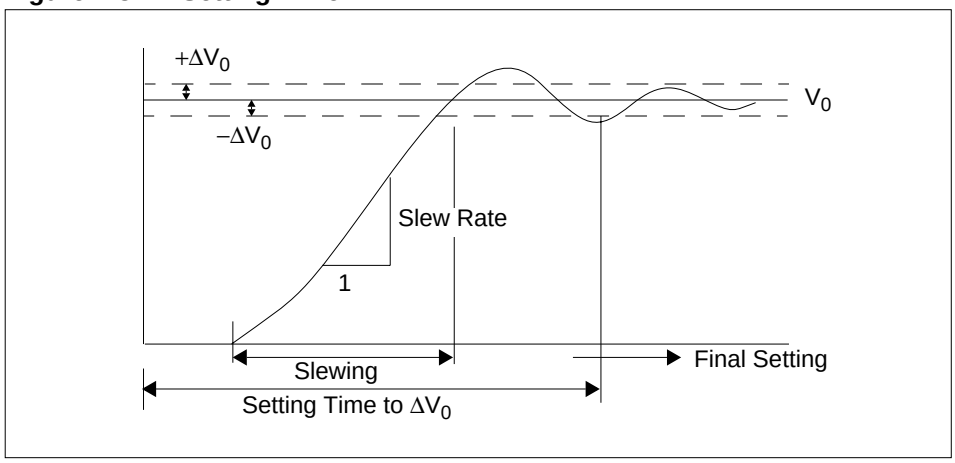
8. Signal-to-Noise Ratio (SNR) - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follows the theoretical formula;

$$S/N_{max} = 6.02N + 1.76\text{dB}$$

9. Slew Rate - Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration such as limited current to charge of capacitor. Amplifiers with slew rate of a few V/μs are common and moderate in cost. Slew rates greater than about 75 V/μs are usually seen only in more sophisticated (and expensive) devices The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

10. Settling Time - The time required, following a prescribed data change from the 50% point of the login input change, for the output of a DAC to reach and to remain within a given fraction (usually ±1/2lsb) of the final value. Typical prescribed changes are full scale, 1MSB and 1LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Figure 1-3. Setting Time



11. Power-Supply Sensitivity -The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (of fractions of 1LSB) for a 1% dc change in the power supply. Power supply sensitivity may also expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed 1/2LSB for 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

12. ILE (integral Linearity Error) - Linearity error of a converter, expressed in %, ppm of full-scale range or multiples of 1LSB, is a deviation of the analog values in a plot of the measured conversion relationship from a straight line. The straight line can be either a "best straight line" determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviation of the actual transfer characteristics from this straight line; or it can be a straight line passing through the endpoints of the transfer characteristic endpoints of the transfer characteristic after they have been calibrated (sometimes referred to as "endpoint" linearity). Endpoint linearity error is similar to relative accuracy error. For multiplying D/A converters, the analog linearity error, at a specified digital code, is defined in the same way as for multipliers, by deviation from a "best straight line" through the plot of the analog output-input response.

13. DLE (Differential Linearity Error) - Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2-n of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called differential linearity error expressed in multiplies of 1LSB. It is an important specification because a differential linearity error greater than 1LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter.

14. Monotonic - A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases with the result that the output will always be a single-valued function of the input. The specification "monotonic"

(over a given temperature range) is sometimes substituted for a differential non-linearity specification since differential nonlinearity less than 1LSB is a sufficient condition for monotonic behaviour.

2. Analog-to-Digital Converter

1. ILE (Integral Linearity Error: INL) - Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB before the first code transition. "Full scale" is defined as a level 1 1/2LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

2. DLE (Differential Linearity Error: DNL) - An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes are guaranteed.

3. Offset Error - The first transition should occur at a level 1/2LSB above "zero". Offset is defined as the deviation of the actual first code transition from that point.

4. Gain Error - The first code transition should occur for an analog value 1/2LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

5. Pipeline Delay (Latency) - The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

6. Effective Number of Bits (ENOB) - This is a measure of a device's dynamic performance and may be obtained from the SNDR or from a sine wave curve test fit according to the following expression:

ENOB = SNDR - 1.76/6.02

ENOB = N-log2[RMS error (actual) / RMS error (ideal)]

7. Analog Bandwidth - The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

8. Aperture Delay - The delay between the sampling clock and the instant the analog input signal is sampled.

9. Aperture Jitter - The sample to sample variation in aperture delay.

10. Bit Error Rate (BER) - The number of spurious code errors produced for any given input sine wave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sine wave.

11. Signal to Noise Ratio - This signal to noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise, and settling time. Over half the sampling frequency, this signal to noise ratio must be specified and should ideally follow the theoretical formula;

$$S/N_{max} = 6.02N + 1.76dB$$

3. Phase Locked Loop

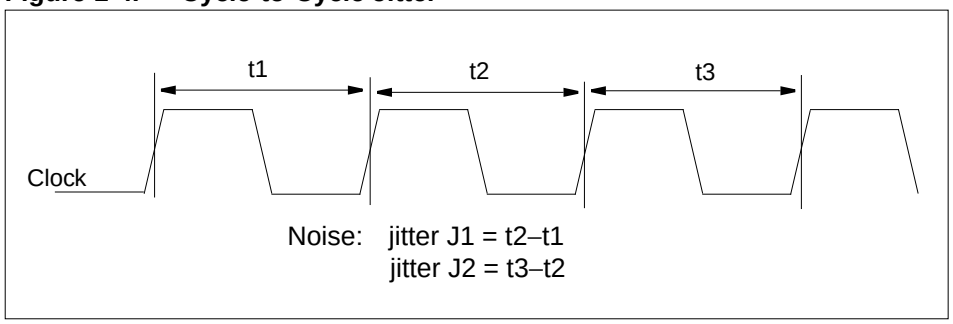
1. Lock Time - The time it takes the PLL to lock onto the system clock. Fast or slow lock time may be controlled by the loop filter characteristics. The loop filter characteristics are controlled by varying the R and C components. (Remember that R and C define the damping-factor as well)

2. Phase Error - The phase difference between the feedback clock signal and the system signal clock.

3. Clock Jitter - The deviations in a clock's output transitions from their ideal positions define the clock jitter. Jitter is sometimes specified as an absolute value in nanoseconds. All jitter measurement are made at a specified voltage.

1) Cycle-to-Cycle Jitter: The change in a clock's output transition from its corresponding position in the previous cycle. This kind of jitter is the most difficult to measure and usually requires a time-interval analyzer

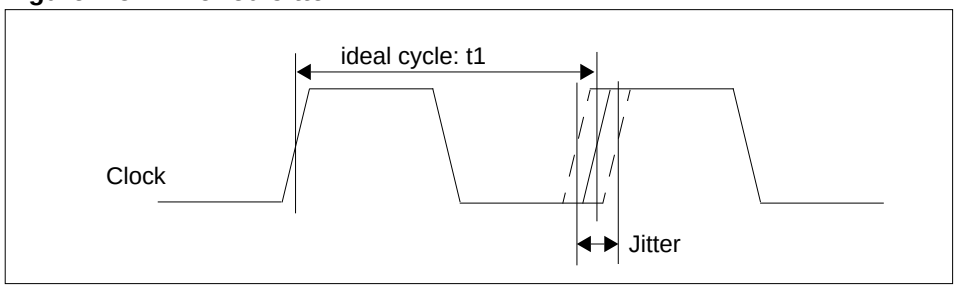
Figure 1-4. Cycle-to-Cycle Jitter



: The maximum of such values over multiple cycles (J1,J2...) is the max. cycle-to-cycle jitter.

2) Period Jitter: Period jitter measures the maximum change in a clock's output transition from its ideal position. You can use period-jitter measurements to calculate timing margins in systems.

Figure 1-5. Period Jitter



3) Long-term Jitter: Long-term jitter measures the maximum change in a clock's output transition from its ideal position over many cycles. How many cycles depends on the application and the frequency. A classic example of system affected by long-term jitter is a graphics card driving a CRT

4) Power Down Mode: PLL state in which the quiescent current is lowered to a very low level to conserve power.

5) Synthesize clock: a system clock may run at a relatively low rate compared to system components. A CPU, for example, may require an internal clock that is several times faster than the system I/O bus clock. Designers can use PLL

technology to synthesize a higher frequency on-chip clock using the system clock as a reference.

6) Deskew clock: Multiple chips on a printed circuit board or cores of different sizes within a single system on a chip experience clock skew. By using PLL or DLL technology to shift the phase of the reference clock within each chip or core, designers can minimize skew tune a system to perform up its potential.

7) Duty Ratio: the percentage of the period that the output is in a high state.

8) Output frequency range: The maximum output frequency range minus the minimum output frequency that is produced with an input signal for which the cell specifications still apply.

Customer Service

SEC provides a full custom support for our customers need of analog cores. SEC's worldwide sales offices and representatives give our customers a first-hand support for analog cores. And if needed, SEC engineers are prepared to provide a fully customized total solution to satisfy our customers.

Technical Support

If our customers want to develop mixed-signal products, SEC provides all technical support to meet customers needs. Mixed-signal design is quite different from pure logic design in terms of circuit design, techniques, layout and test methodology. Thus SEC provides a successful technical guide and firmly support for all development steps.

Definition of Analog Core Data Sheet Types

Each product developed by SEC will be supported by technical literature where the data sheets progress through the following levels of refinement

1. Core Preview

Describes the main features and specifications for core that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication.The purpose of this document is to provide customers with advance product planning information.

2. Preliminary Datasheet

This is the first document completely describing a new core. It contains an features, application, timing diagram, theory of operation, core pin information, test guide, layout guide and AC/DC electrical information. This data sheet are based on prototype silicon performance and on worst case simulation models.The purpose of this data sheet is to provide ASIC customer with technical information sufficiently detailed to guarantee that they can safely begin active development.

3.Final Data sheet

This is an updated version of preliminary data sheet reflecting actual performance of the final silicon. Updates include tighter specifications, more min. and max. values. The purpose of this data sheet is to communicate the confirmed performance of cores which have passed qualification, been fully characterized.

1.4.2 INTERNAL MACROCELLS

Internal Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 471 different types of internal macrocells. They usually come in four levels of drive strength (0.5X, 1X, 2X and 4X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

1.4.3 COMPILED MACROCELLS

Compiled macrocells of STD110 consist of compiled memory and compiled datapath macrocells.

1.4.3.1 Compiled Memory Macrocells

Memories in STD110 are fully user-configurable and are provided as a compiler. Two different types of memories are available in STD110. One is suitable for high-density application with high-performance, called STD110-HD compiled memory. The other is suitable for low-power application, called STD110-LP compiled memory.

In STD110-HD compiled memory, eight types of memories are available such as single-port synchronous/asynchronous static RAM, dual-port synchronous static RAM, synchronous diffusion/metal-programmable ROM, multi-port asynchronous register file and synchronous first-in first-out memory. Synchronous memories have a fully synchronous operation at the rising-edge of clock and the duty-free cycle is available. Also, the bit-write capability is available. Asynchronous memories have a synchronous operation for a write enable signal during write mode and have an asynchronous operation for address signal during read mode. Multi-port asynchronous register file supports four kinds of configurations such as 2 port(1-read/1-write), 3 port(1-read/2-write and 2-read/1-write) and 4 port (2-read/2-write). The first-in first-out memory which is widely used in communication buffering types of applications has also fully synchronous operation at the rising- edge of clock.

On the other hand, in STD110-LP compiled memory, five types of memories are available such as single-port synchronous/asynchronous static RAM, dual-port synchronous static RAM and synchronous diffusion/metal-programmable ROM. Synchronous memories are almost same as that of STD110-HD except that the duty-free cycle is not available. Asynchronous memory is same as that of STD110-HD.

To dramatically reduce the power consumption in STD110-LP, some of low-power techniques such as a partial activation architecture in cell array and a divided word-line structure was adopted, rather than STD110-HD.

Basically in STD110-HD and STD110-LP, the power-down mode which significantly reduces the power dissipated during a read or write mode is provided. Also compiled memories have a standby mode except multi-port asynchronous register file and first-in first-out memory. While in standby mode, the data stored in the memory is retained, data outputs remain stable and the power is greatly reduced because memory operation is internally blocked while the memory contents and the data outputs are unaffected.

To improve the memory performance and to reduce the power consumption, 2-bank architecture is provided except some memories such as dual-port synchronous static RAM, multi- port asynchronous register file and first-in first-out memory. In 2-bank architecture, only one bank is activated and the other bank is in standby mode.

To support various memory shapes which are determined by the floorplan of a chip design, flexible memory aspect ratios are provided. For certain specific memory configuration, all types of timing, power and area values are provided by an automatic datasheet generator.

To easily do interface to layout, the physical abstract data for Silicon Ensemble and Apollo, called phantom cell or black box, is provided. BIST(Built-In Self-Test) circuitry is currently available for most of STD110 compiled memories. BIST circuits are designed to detect a set of fault types that impact the functionality of memory and is generated by a softmacro-based BIST generator.

The softmacro-based BIST generator generates both an individual BIST netlist for each memory and a shared BIST netlist for all memories used in a design. However, when several memories of the same or the different type area used in the design, if you generate the individual BIST netlist for each memory, there are some redundant blocks because the individual BIST netlist has same function. In this case, it would better use the shared BIST netlist to eliminate such redundancy and reduce area.

1.4.3.2 Compiled Datapath Macrocells

Compiled datapath macro cells include Adder, Barrel Shifter and Multiplier. Adder performs the adding or adding/subtracting operation on the control of a mode selection signal. Barrel Shifter makes input data shift or rotate in the left/right direction. In the shift operation, the vacant bit can be padded with zero, MSB value, or external data. Multiplier performs the 2's compliment multiplication. One pipeline stage insertion is available to get a high operating frequency.

They have two output drive strengths, which are equal to the 1X and 2X-Drive in the primitive cell library. The hard macro cells are built through the Apollo, placement and routing tool from Avant!. All the leaf cells have the same physical configuration compatible with the primitive cell library. It allows that any primitive cell can be used as a bit slice cell in the datapath module design.

We provide two kinds of engineering design services. One is to support additional compiled datapath macrocells such as ALUs, Comparators, Priority encoders, Incrementers and Decrementers, and so on. Another is to make hardwired datapath module design which provides a regular structured layout.

1.4.4 INPUT/OUTPUT CELLS

There are about seven hundreds different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of a chip.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including LVCMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 12mA for 2.5V, 3.3V drive and from 1mA to 3mA for 5.0V tolerant drive. One or two levels of slew rate controls are provided for each buffer type (except 1mA, 2mA and 3mA buffers) to reduce output power/ground noise and signal ringing, especially in simultaneous switching outputs.

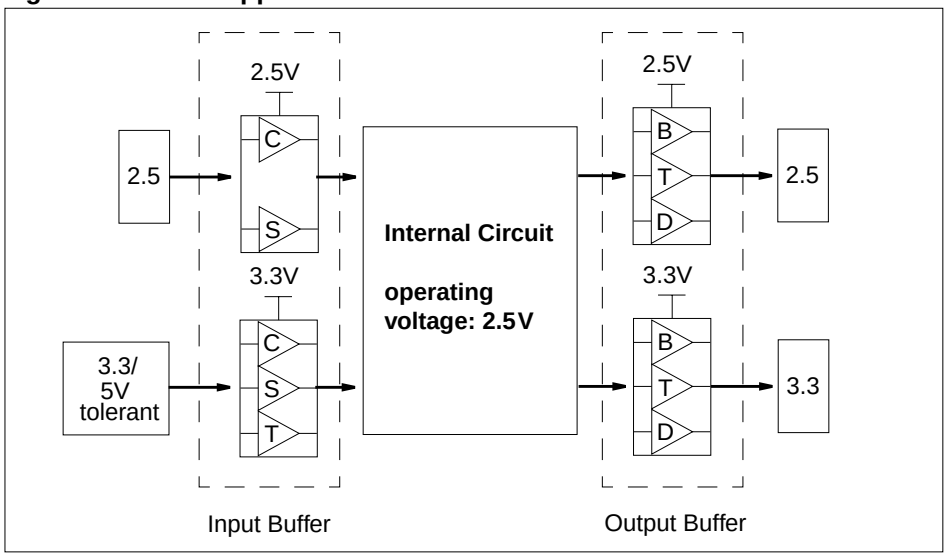
Bi-directional buffers are combinations of input buffers and output buffers (tri-state and open drain) in a single unit. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STD110 library provides 100KΩ pull-down and pull-up resistance respectively.

1.4.4.1 I/O Applications

To support mixed voltage environments, LVTTL, LVCMOS and Schmitt trigger I/O cells are available at 2.5V, 3.3V interface and 5V tolerant interface. The I/O application diagram is as follows.

Figure 1-6. I/O Applications



1.4.4.2 I/O Cell Drives Options

To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA,..., 12mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells.

STD110 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

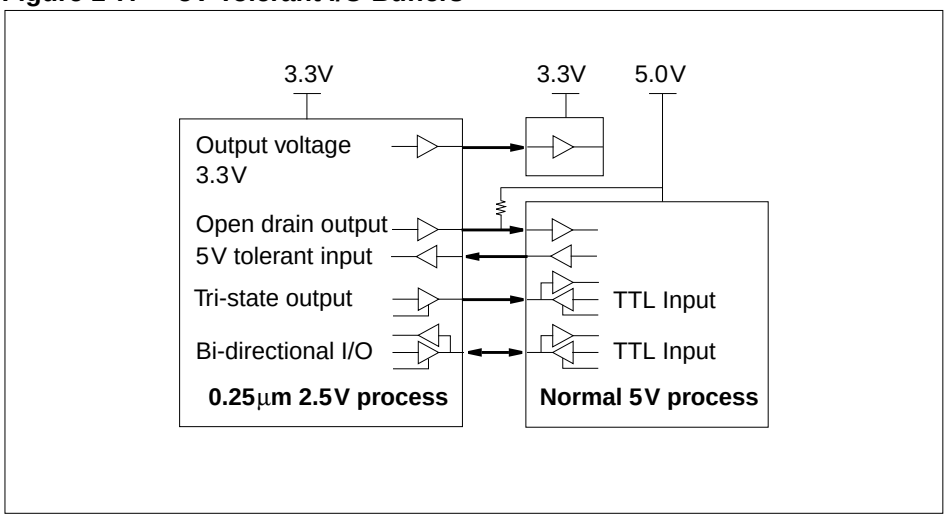
1.4.4.3 5V Tolerant I/O Buffers

STD110 I/O library is based on a process which has the most optimum performance in 2.5V.

In this process, voltage more than 3.6V are not allowed at the gate oxide because of a reliability problem. And a special circuit is adopted in order to make pin voltage tolerable up to 5.25V and to offer TTL interface driving up to 3mA. Obviously, this circuit is constructed not to permit more than 3.6V at the gate oxide. The external circuit diagram is as follows.

The maximum external tolerance of this buffer is 5.25V. It can be used as a 3.3V normal buffer.

Figure 1-7. 5V Tolerant I/O Buffers



1.4.4.4 PCI Buffers

PCI buffers are designed for PCI local bus application which is an industry-standard, high-performance 32bit or 64bit bus architecture. SEC ASIC offers input, output, bi-directional PCI buffers for 33MHz and 66MHz operation. These buffers are compliant with PCI local bus specification 2.1.

1.4.4.5 USB (Universal Serial Bus) Buffers

Various kinds of peripheral equipment such as mouse, joy stick, keyboard, modem, scanner and printer improve the power of a computer. However, it is not easy to connect and use them properly in the computer.

USB specification established late in 1995 is a good solution for this problem, providing facile method of an expansion. SEC ASIC offers full speed and low speed USB buffers that complies with Universal Serial Bus specification 1.0, 1.1.

1.4.4.6 Other Buffers

SEC ASIC can support various kinds of buffers such as HSTL, SSTL, AGP, PECL, LVDS, and so on. For more information please contact us.

1.5 Timings

1.5.1 WIRE LENGTH LOAD

Table 1-1. shows the equivalent standard load matrix for 4-layer and 5-layer metal interconnect. The equivalent standard load values are function of gate count and fanout. These values are based on capacitive loading and are used in wire length estimates which affect propagation delay.

Table 1-1. Equivalent Standard loads for 4-layer and 5-layer Metal Interconnect

Gates Count	Fanouts										
	1	2	3	4	5	6	7	8	16	32	64
4LM											
5000	1.159	2.242	3.822	5.113	5.965	7.020	7.859	10.94	28.672	45.642	79.821
10000	1.530	2.932	5.561	7.701	8.964	10.500	12.110	15.211	29.903	47.725	83.520
50000	4.192	8.247	12.439	16.494	16.801	17.980	21.026	22.806	35.536	48.347	84.605
100000	4.596	9.327	13.925	18.523	18.889	20.241	23.582	27.031	41.002	54.253	94.944
150000	12.843	17.125	21.406	22.684	23.600	24.296	26.001	29.730	39.828	63.672	127.344
200000	13.520	18.026	22.533	23.885	24.849	25.582	27.372	31.299	41.865	66.931	133.812
300000	14.871	19.830	24.786	26.588	27.596	28.363	30.317	34.634	46.268	73.871	147.587
400000	16.225	21.631	26.852	28.693	29.845	30.718	32.868	37.479	50.016	79.707	159.207
500000	18.099	24.132	30.166	32.177	33.435	34.390	36.777	42.032	53.235	84.861	169.459
600000	19.375	25.836	32.476	34.593	35.915	36.919	39.467	45.186	54.763	87.312	174.320
800000	22.324	29.767	37.739	40.113	41.593	42.719	45.642	52.399	59.180	94.390	188.385
1000000	25.078	33.439	42.657	45.272	46.898	48.140	51.408	59.135	63.283	100.964	201.447
1500000	32.631	43.509	56.047	59.341	61.381	62.946	67.174	77.514	75.639	120.743	240.788
2000000	39.706	52.941	68.596	72.524	74.956	76.821	81.946	94.736	87.196	139.244	277.587
2500000	46.327	61.770	80.342	84.864	87.657	89.807	95.771	110.853	97.994	156.527	311.959
3000000	52.517	70.023	91.321	96.399	99.532	101.946	108.693	125.919	108.065	172.646	344.022
4000000	60.251	80.335	104.770	110.594	114.189	116.958	124.701	144.463	123.979	198.073	394.685
5000000	67.558	90.078	117.479	124.008	128.041	131.146	139.827	161.985	139.017	222.099	442.560
6000000	75.754	101.005	131.728	139.052	143.573	147.053	156.788	181.634	155.879	249.038	496.241
5LM											
5000	1.101	2.131	3.631	4.856	5.667	6.669	7.466	10.397	27.238	43.360	75.830
10000	1.454	2.786	5.283	7.317	8.515	9.976	11.505	14.451	28.408	45.339	79.344
50000	3.982	7.834	11.818	15.670	15.961	17.081	19.976	21.666	33.760	45.929	80.374
100000	4.366	8.861	13.229	17.597	17.944	19.229	22.403	25.679	38.952	51.540	90.198
150000	12.201	16.268	20.336	21.549	22.420	23.081	24.701	28.244	37.837	60.488	120.977
200000	12.843	17.125	21.406	22.691	23.606	24.304	26.004	29.734	39.771	63.584	127.122
300000	14.128	18.839	23.546	25.259	26.216	26.944	28.801	32.903	43.955	70.178	140.207
400000	15.414	20.549	25.509	27.257	28.353	29.181	31.225	35.606	47.515	75.722	151.247
500000	17.195	22.925	28.658	30.567	31.763	32.670	34.938	39.931	50.573	80.618	160.986
600000	18.406	24.543	30.852	32.862	34.119	35.073	37.494	42.926	52.025	82.947	165.605
800000	21.208	28.278	35.852	38.107	39.514	40.584	43.360	49.779	56.220	89.670	178.967
1000000	23.825	31.767	40.524	43.008	44.554	45.733	48.837	56.178	60.119	95.916	191.374
1500000	31.000	41.333	53.245	56.374	58.312	59.798	63.815	73.637	71.856	114.706	228.749
2000000	37.721	50.295	65.166	68.898	71.208	72.980	77.849	90.000	82.837	132.281	263.707
2500000	44.011	58.682	76.324	80.621	83.274	85.317	90.983	105.311	93.093	148.700	296.362
3000000	49.891	66.523	86.755	91.579	94.555	96.849	103.257	119.622	102.661	164.014	326.821
4000000	57.239	76.318	99.532	105.065	108.479	111.110	118.466	137.239	117.779	188.169	374.950
5000000	64.180	85.575	111.606	117.807	121.639	124.588	132.836	153.885	132.067	210.995	420.432
6000000	71.965	95.955	125.141	132.099	136.394	139.700	148.949	172.552	148.084	236.587	471.429
7000000	78.436	104.582	136.393	143.976	148.655	152.259	162.339	188.067	161.397	257.858	513.812
8000000	87.950	117.266	152.935	161.439	166.687	170.727	182.031	210.877	180.976	289.134	576.135

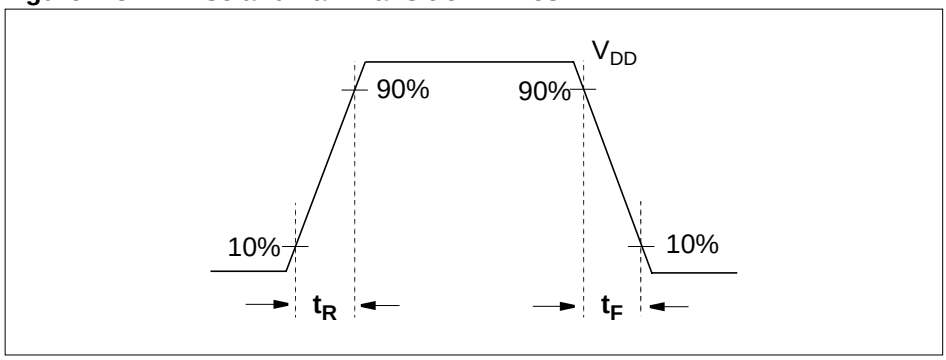
1.5.2 TIMING PARAMETERS

This section discusses issues involving timing parameters.

1.5.2.1 Transition Time

Figure 1-8. shows the definition of rise transition time (t_R) and fall transition time (t_F). Transition time is defined as the delay between the time when the input (output) signal voltage level is 10% of supply voltage (V_{DD}) and the time of the input (output) signal voltage level is 90% of V_{DD}.

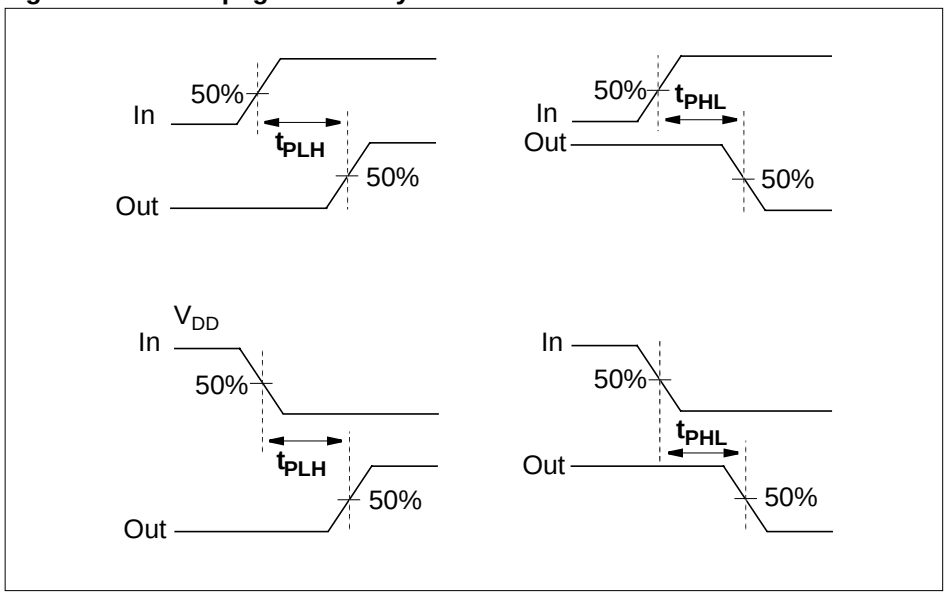
Figure 1-8. Rise and Fall Transition Times



1.5.2.2 Propagation Delays

Figure 1-9. shows the definition of propagation delays. Propagation delay is defined as the delay between the time when the input signal voltage level is 50% of supply voltage (V_{DD}) and the time when the output signal voltage level is 50% of V_{DD}.

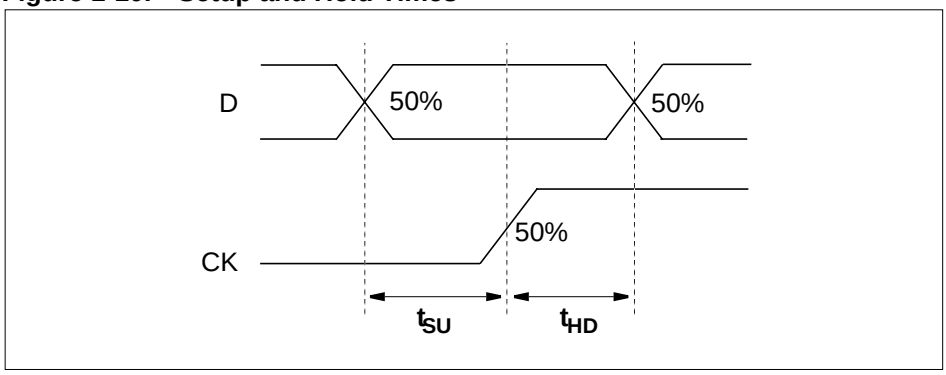
Figure 1-9. Propagation Delay



1.5.2.3 Setup / Hold Time

Figure 1-10. shows the definition of setup time and hold time. The setup timing check is defined as the minimum interval which a data signal must remain stable before active transition of a clock. Any change to the data signal within this interval results in a timing violation.
The hold timing check is defined as the minimum interval which a data signal must remain stable after active transition of a clock. Any change to the data signal within this interval results in a timing violation.

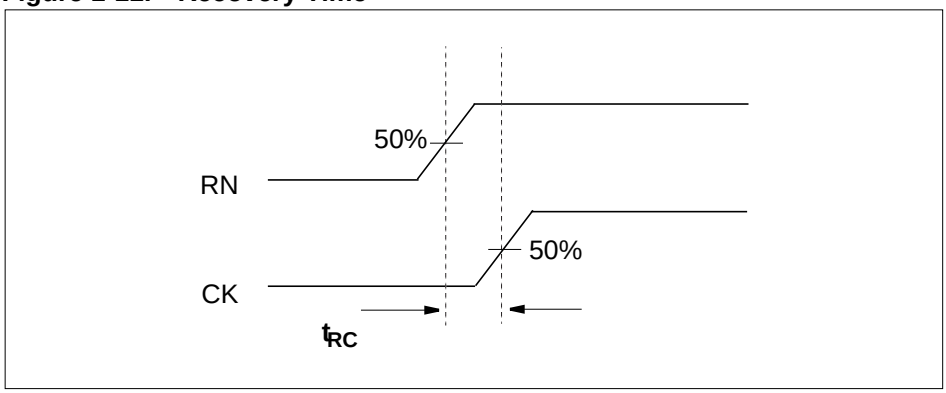
Figure 1-10. Setup and Hold Times



1.5.2.4 Recovery Times

Figure 1-11. shows the definition of recovery time. A recovery timing check measures the time between the release of an asynchronous control signal from the active state to the next active clock edge.
For example, the time between RN and the CK of FD2 cell. If the active edge of the CK occurs too soon after the release of the RN, the state of the FD2 becomes uncertain. The state can be the value set by the RN or the value clocked into the FD2 from the data input.

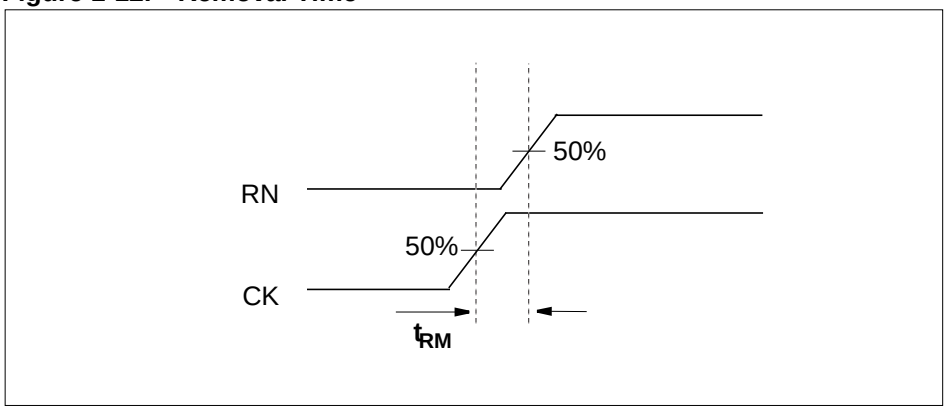
Figure 1-11. Recovery Time



1.5.2.5 Removal Times

Figure 1-12. shows the definition of removal time. A removal timing check measures the time between the active clock edge and the release of an asynchronous control signal from the active state.
For example, the time between RN and the CK of FD2 cell. If the release of the RN occurs too soon after the active edge of the clock, the state of the FD2 becomes uncertain. The uncertainty can be caused by the value set by the RN or the value clocked into the FD2 from the data input.

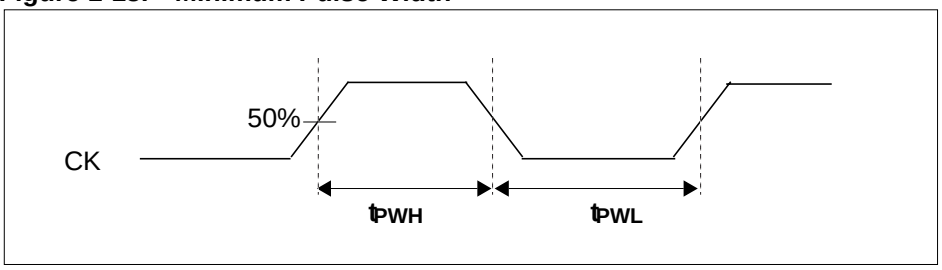
Figure 1-12. Removal Time



1.5.2.6 Minimum Pulse Widths

Figure 1-13. shows the definition of minimum pulse width. The minimum pulse width timing check is the minimum allowable time for the positive (high) or negative (low) phase of each cycle.

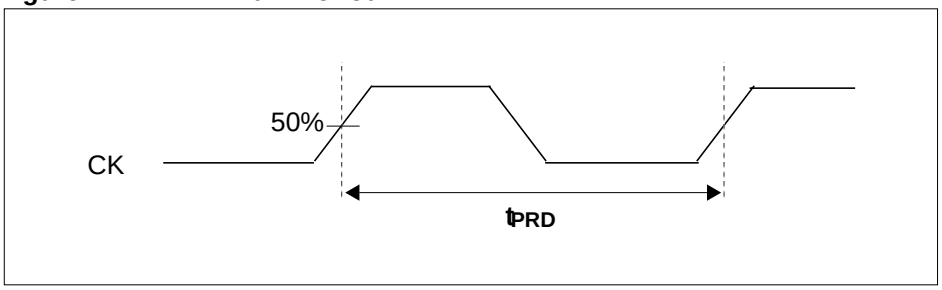
Figure 1-13. Minimum Pulse Width



1.5.2.7 Minimum Period

Figure 1-14. shows the definition of minimum period. The minimum period timing check is the minimum allowable time for one complete cycle of the signal.

Figure 1-14. Minimum Period

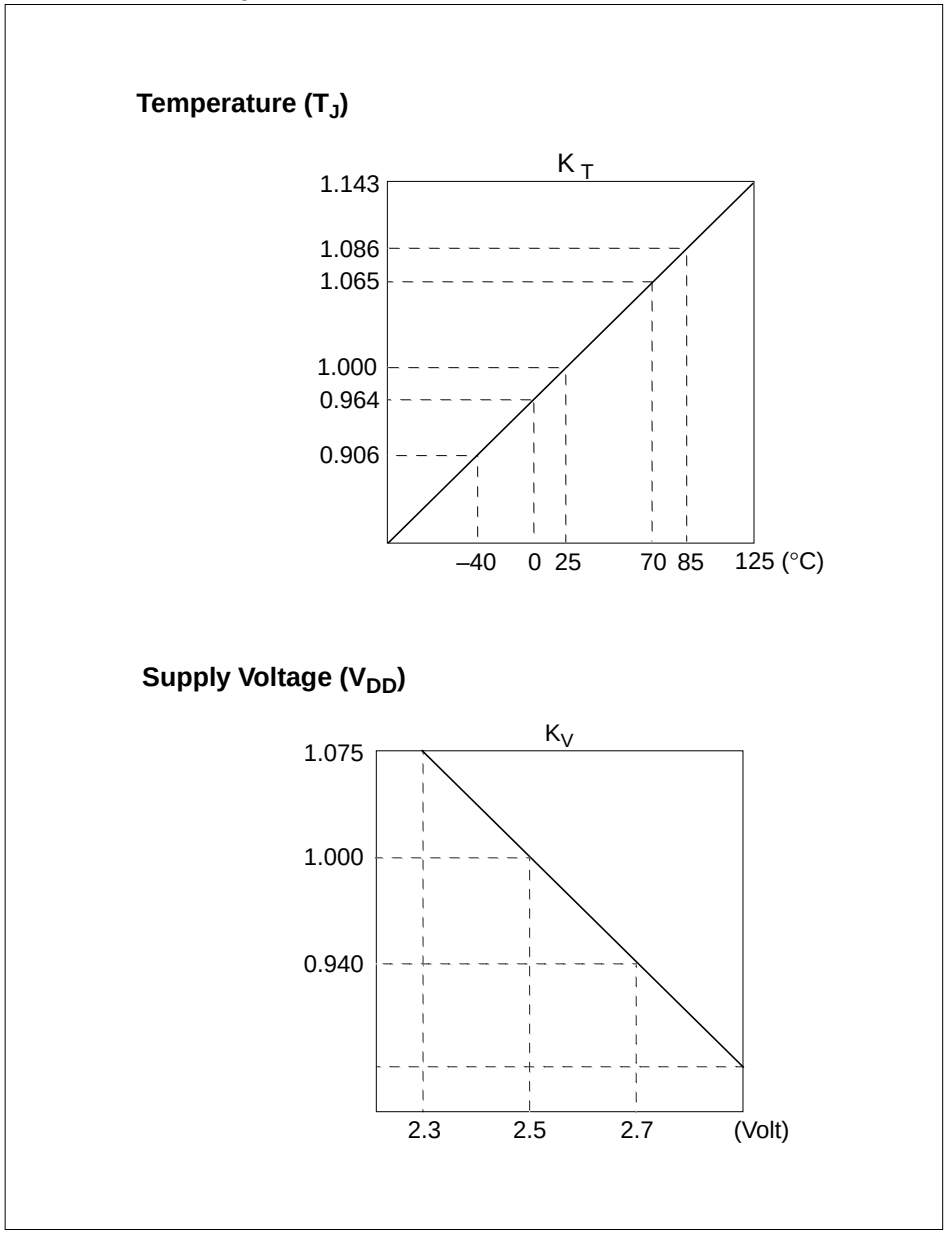


1.5.3 TEMPERATURE AND SUPPLY VOLTAGE

The next figure describes propagation delay derating factors (K_T, K_V) as a function of on-chip junction temperature (T_J) and supply voltage (V_{DD}). As a result of power dissipation, the junction temperature is generally higher than the ambient temperature.

The temperature of the die inside the package (junction temperature, T_J) is calculated using chip power dissipation and the thermal resistance to the ambient temperature (θ_{JA}) of the package. Information on package thermal performance can be obtained from SEC application engineers.

Figure 1-15. Effect of Temperature and Supply Voltage on Propagation Delay



1.5.4 BEST AND WORST CASE CONDITIONS

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case(Worst case):

T_{BC} (T_{WC}) = K_P x K_T x K_V x T_{NOM}

where

$\boldsymbol{T}_{BC}$ = Best case propagation delay

$\boldsymbol{T}_{WC}$ = Worst case propagation delay

T_{NOM} = Normal propagation delay

($\boldsymbol{T}_J$ = 25^{o}C, $\boldsymbol{V}_{DD}$ = 2.5V and typical process)

$\boldsymbol{K}_P$, $\boldsymbol{K}_T$, $\boldsymbol{K}_V$ = Refer toTable 1-2., Table 1-3., and Table 1-4.

1.5.5 DERATING FACTORS OF STD110

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of V_{DD} = 2.5V, T_J = 25°C and typical process.

The derating factors of STD110 is as follows.

Table 1-2. STD110 cell process derating factor (K_P)

Process Factor (K_P)	Slow	Typ	Fast
	1.212	1.0	0.841

Table 1-3. STD110 cell temperature derating factor (K_T)

Temp. (^{o}C)	125	85	70	25	0	–40
K_T	1.143	1.086	1.065	1.000	0.964	0.906

Table 1-4. STD110 cell voltage derating factor (K_V)

Voltage (V)	2.3	2.5	2.7
K_V	1.075	1.000	0.940

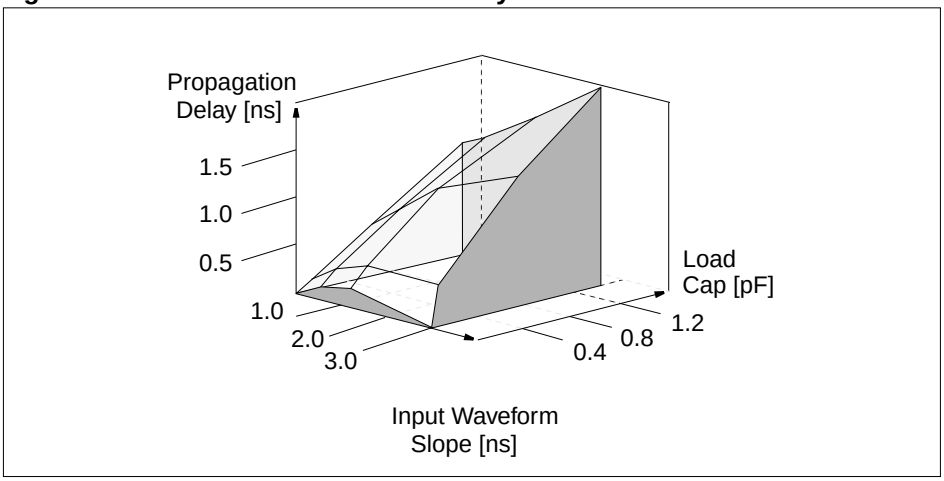
1.6 Delay Model

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for STD110 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. SEC ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.25μm cell-based products.

Figure 1-16. 2-Dimensional Table Delay Model



The Table 1-5. shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

Table 1-5. Table Delay Model Example

SLOP \ CAP	0.0050	0.0220	0.3030	0.5840
0.0200	0.03644	0.07275	0.66481	1.25660
0.1700	0.05508	0.09725	0.68658	1.27820
1.5850	0.07719	0.16698	0.92337	1.49790
3.0000	0.06421	0.17730	1.10970	1.74950

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The figure below summarizes the features of SEC ASIC's delay model.

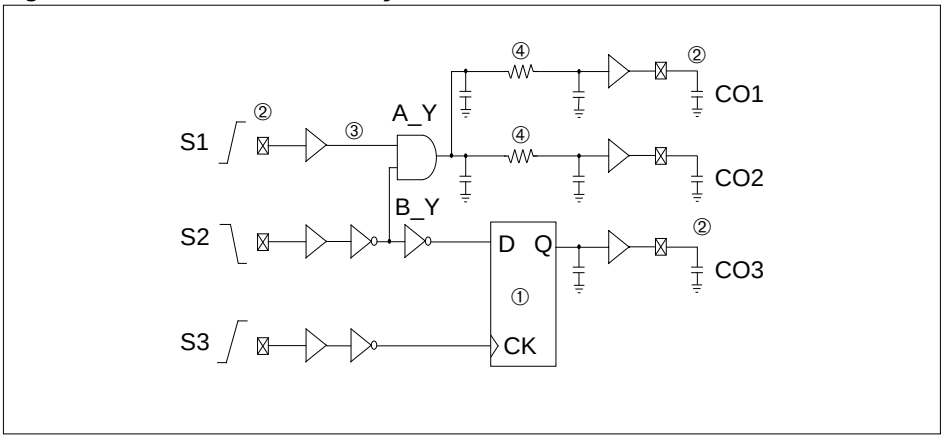
① 2-dimensional table delay model for output loading and input waveform slope effects is used.The slopes (t_R, t_F) and delay times (t_{PLH}, t_{PHL}) of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are supported.

④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

Figure 1-17. Features of Delay Model



1.7 Testability Design Methodology

1.7.1 SCAN DESIGN

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design.
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

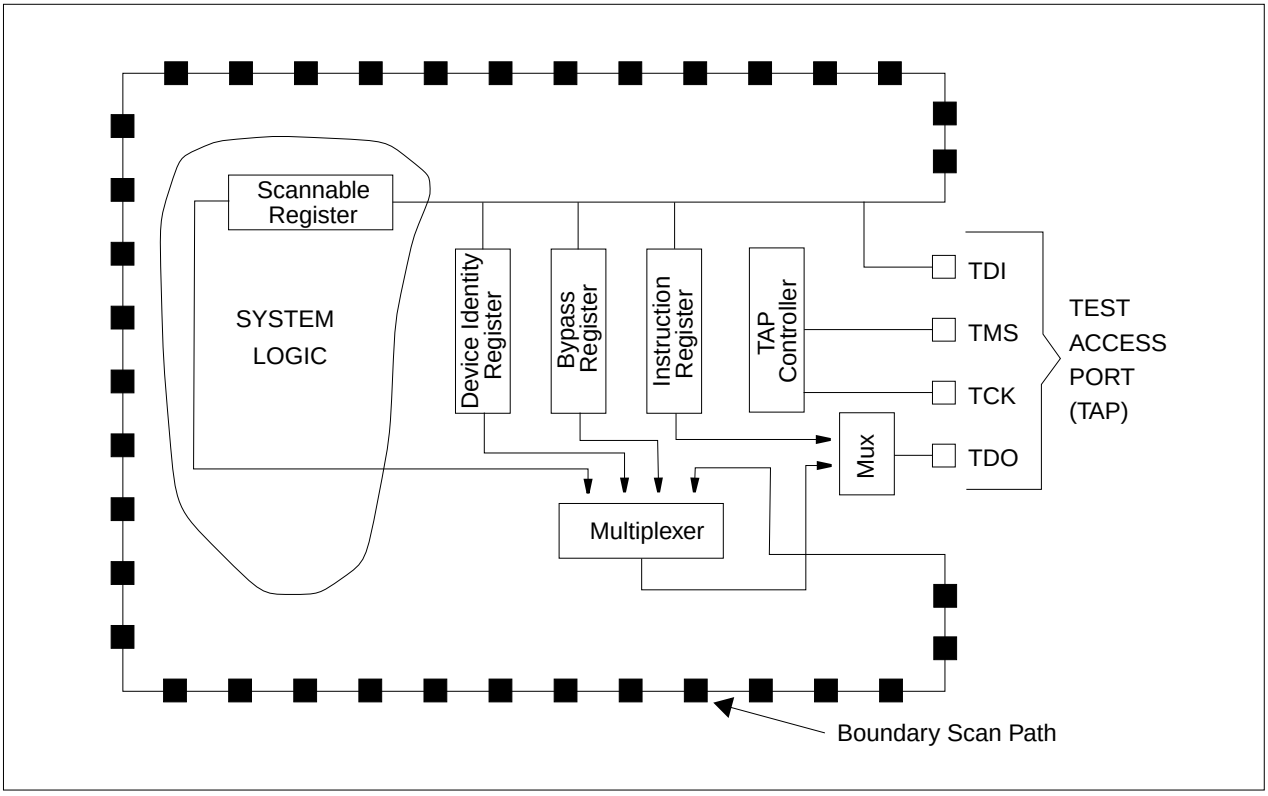
1.7.2 BOUNDARY-SCAN

- IEEE Std 1149.1
- JTAG boundary-scan registers with primitive cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design and core testing

Boundary Scan Architecture

A boundary scan architecture contains TAP (Test Access Port), TAP controller, instruction register and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output which are connected to TAP, TDI and TDO signals. TAP controller selects the alternative instruction and test data register paths between TDI and TDO. The schematic view of the top level design of the test logic architecture is shown in the Figure 1-18.

Figure 1-18. JTAG Test Access Port (TAP) Block Diagram



Boundary Scan Functional Block Descriptions

TAP (Test Access Port)

TAP is a general-purpose port that can provide with an access to many test support functions built into a component, including the test logic. It includes three inputs (TCK; Test Clock Signal, TMS; Test Mode Signal and TDI; Test Data Input) and one output (TDO; Test Data Output) required by the test logic. An optional fourth input (TRSTN; Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO pin changes on the falling edge of TCK.

TAP Controller

TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuitries as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include a selection of tests to be performed or the test data register to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass- and boundary scan registers are mandatory; the rest are optional.

Bypass register: The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers is selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.

Boundary scan register: The boundary scan register detects typical production defects in board interconnects, such as opens, shorts, etc. It also allows an access to component inputs and outputs when you test their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose. These special registers is discussed in the next section of next pages.

Design-specific test data register: These optional registers may be provided to allow an access to design-specific test support features in the integrated circuit, such as self-test, scan test.

Device identification register: This is an optional test data register that allows the manufacturer part number and variant of a components to be identified. The 32-bit identification register is partitioned into four fields:

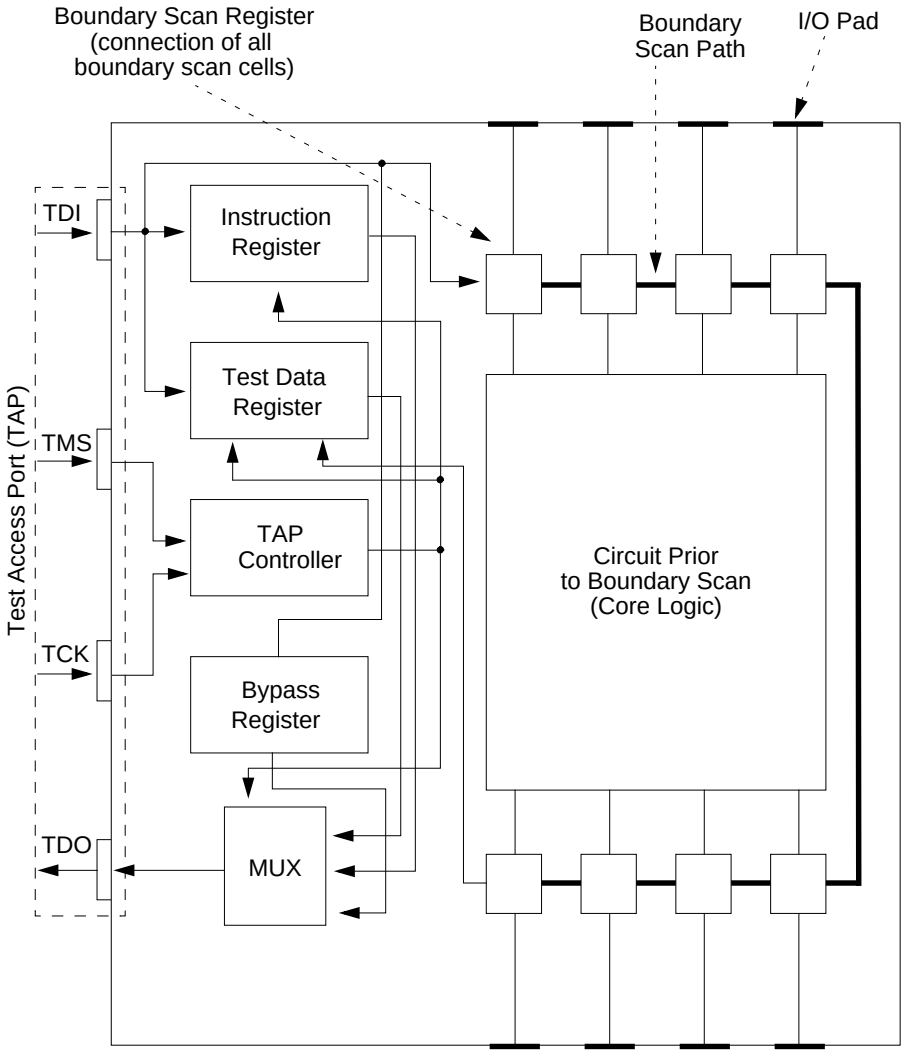
Device version identifier1st field	The first four bits beginning from MSB	
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit —tied in High

The ASIC designer is free to fill the version and part number in any manner as long as the total twenty bits are used.

SEC's JEDEC code: 78 decimal = 1001110
Continuation field (4 bits) = 0000

Contents of device identification register:

XXXX XXXXXXXXXXXXXXX 0000 1001110 1
Users can define these two fields.



1.7.3 BIST (BUILT-IN SELF-TEST)

- Efficient test solution for compiled memory macrocells
- At speed and parallel testing of multiple memories
- Less routing overhead and test pin requirements

1.8 Maximum Fanouts

1.8.1 INTERNAL MACROCELLS

The maximum fanouts for STD110 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.213ns. Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STD110 internal macrocells are listed.

Table 1-6. Maximum Fanouts of Internal Macrocells
(When input t_R/t_F = 0.213ns, one fanout (SL) = 0.006710pF**)**

Cell Name	Output Pin	Maximum Fanouts
ad2	Y	48
ad2d2	Y	97
ad2d4	Y	190
ad2dh	Y	21
ad3	Y	48
ad3d2	Y	94
ad3d4	Y	188
ad3dh	Y	21
ad4	Y	48
ad4d2	Y	94
ad4d4	Y	185
ad4dh	Y	21
ad5	Y	23
ad5d2	Y	46
ad5d4	Y	190
ao21	Y	22
ao211	Y	14
ao2111	Y	9
ao2111d2	Y	97
ao211d2	Y	28
ao211d2b	Y	97
ao211d4	Y	195
ao211dh	Y	7
ao21d2	Y	45
ao21d2b	Y	95
ao21d4	Y	192
ao21dh	Y	10
ao22	Y	22
ao221	Y	13
ao221d2	Y	95
ao221d4	Y	192
ao222	Y	13
ao2222	Y	8
ao2222d2	Y	95
ao2222d4	Y	192
ao222a	Y	20
ao222d2	Y	25
ao222d2a	Y	95
ao222d2b	Y	95
ao222d4	Y	191
ao222d4a	Y	192
ao22a	Y	22
ao22d2	Y	43
ao22d2a	Y	43
ao22d2b	Y	96
ao22d4	Y	191
ao22d4a	Y	191
ao22dh	Y	9
ao22dha	Y	9
ao31	Y	21
ao311	Y	13
ao3111	Y	8
ao3111d2	Y	97
ao311d2	Y	97
ao311d4	Y	191
ao31d2	Y	43
ao31d4	Y	194
ao31dh	Y	9
ao32	Y	20
ao321	Y	12
ao321d2	Y	95
ao321d4	Y	192
ao322	Y	11
ao322d2	Y	95
ao322d4	Y	192
ao32d2	Y	97
ao32d4	Y	191
ao33	Y	19
ao331	Y	11
ao331d2	Y	95
ao331d4	Y	193
ao332	Y	10
ao332d2	Y	95
ao332d4	Y	192
ao33d2	Y	95
ao33d4	Y	190
ao4111	Y	8
ao4111d2	Y	95
busholder	Y	10000
dc4	Y0	47
	Y1	47
	Y2	47
	Y3	47
dc4i	YN0	43
	YN1	43
	YN2	44
	YN3	44
dc8i	YN0	30
	YN1	30
	YN2	30
	YN3	30
	YN4	30
	YN5	30
	YN6	30
	YN7	30
dl1d2	Y	96
dl1d4	Y	195
dl2d2	Y	97
dl2d4	Y	197
dl3d2	Y	96
dl3d4	Y	194
dl4d2	Y	95
dl4d4	Y	194
dl5d2	Y	96
dl5d4	Y	194
dl10d2	Y	96
dl10d4	Y	194

Cell Name	Output Pin	Maximum Fanouts
oak_duclk10	CK	359
	CKB	358
oak_duclk16	CK	359
	CKB	359
fa	S	47
	CO	46
fad2	S	96
	CO	96
fadh	S	20
	CO	20
fd1	Q	47
	QN	47
fd1d2	Q	95
	QN	95
fd1cs	Q	47
	QN	47
fd1csd2	Q	95
	QN	95
fd1q	Q	48
fd1qd2	Q	95
fd1s	Q	47
	QN	47
fd1sd2	Q	97
	QN	95
fd1sq	Q	47
fd1sqd2	Q	95
fd2	Q	47
	QN	48
fd2d2	Q	95
	QN	95
fd2cs	Q	48
	QN	47
fd2csd2	Q	97
	QN	94
fd2q	Q	48
fd2qd2	Q	95
fd2s	Q	46
	QN	48
fd2sd2	Q	95
	QN	95
fd2sq	Q	47
fd2sqd2	Q	95
fd3	Q	48
	QN	48
fd3d2	Q	103
	QN	103
fd3cs	Q	47
	QN	48
fd3csd2	Q	95
	QN	94
fd3q	Q	47
fd3qd2	Q	95
fd3s	Q	48
	QN	48
fd3sd2	Q	95
	QN	95
fd3sq	Q	47
fd3sqd2	Q	95
fd4	Q	47
	QN	48
fd4d2	Q	95
	QN	94
fd4cs	Q	46
	QN	45

Cell Name	Output Pin	Maximum Fanouts
fd4csd2	Q	97
	QN	91
fd4q	Q	47
fd4qd2	Q	95
fd4s	Q	47
	QN	46
fd4sd2	Q	95
	QN	94
fd4sq	Q	47
fd4sqd2	Q	94
fd5	Q	47
	QN	47
fd5d2	Q	95
	QN	95
fd5s	Q	47
	QN	47
fd5sd2	Q	97
	QN	95
fd6	Q	47
	QN	48
fd6d2	Q	95
	QN	95
fd6s	Q	46
	QN	47
fd6sd2	Q	95
	QN	95
fd7	Q	48
	QN	48
fd7d2	Q	95
	QN	95
fd7s	Q	47
	QN	48
fd7sd2	Q	95
	QN	95
fd8	Q	47
	QN	46
fd8d2	Q	95
	QN	94
fd8s	Q	48
	QN	48
fd8sd2	Q	95
	QN	94
fds2	Q	47
	QN	46
fds2d2	Q	95
	QN	95
fds2cs	Q	47
	QN	46
fds2csd2	Q	95
	QN	95
fds2s	Q	47
	QN	48
fds2sd2	Q	95
	QN	95
fds3	Q	47
	QN	47
fds3d2	Q	95
	QN	95
fds3cs	Q	48
	QN	47
fds3csd2	Q	95
	QN	95
fds3s	Q	46
	QN	48

Cell Name	Output Pin	Maximum Fanouts
fds3sd2	Q	95
	QN	95
fj1	Q	47
	QN	48
fj1d2	Q	95
	QN	95
fj1s	Q	46
	QN	48
fj1sd2	Q	95
	QN	95
fj2	Q	46
	QN	47
fj2d2	Q	95
	QN	95
fj2s	Q	46
	QN	48
fj2sd2	Q	95
	QN	95
fj4	Q	47
	QN	47
fj4d2	Q	94
	QN	96
fj4s	Q	48
	QN	47
fj4sd2	Q	95
	QN	93
ft2	Q	48
	QN	48
ft2d2	Q	94
	QN	94
ha	S	47
	CO	47
had2	S	94
	CO	95
hadh	S	21
	CO	21
iv	Y	48
ivcd11	Y	46
	YN	47
ivcd13	Y	43
	YN	144
ivcd22	Y	94
	YN	97
ivcd26	Y	87
	YN	284
ivcd44	Y	191
	YN	196
ivd2	Y	97
ivd3	Y	144
ivd4	Y	195
ivd6	Y	282
ivd8	Y	381
ivd16	Y	787
ivdh	Y	21
ivt	Y	41
ivtd2	Y	89
ivtd4	Y	187
ivtd8	Y	373
ivtd16	Y	756
ivtn	Y	41
ivtnd2	Y	89
ivtnd4	Y	187
ivtnd8	Y	373
ivtnd16	Y	757

Cell Name	Output Pin	Maximum Fanouts
ld1	Q	47
	QN	46
ld1d2	Q	95
	QN	95
ld1a	Q	35
ld1d2a	Q	77
ld1q	Q	47
ld1qd2	Q	95
ld2	Q	46
	QN	47
ld2d2	Q	95
	QN	95
ld2q	Q	47
ld2qd2	Q	95
ld3	Q	47
	QN	47
ld3d2	Q	95
	QN	95
ld4	Q	48
	QN	46
ld4d2	Q	97
	QN	96
ld5	Q	47
	QN	47
ld5d2	Q	95
	QN	95
ld5q	Q	47
ld5qd2	Q	95
ld6	Q	46
	QN	47
ld6d2	Q	95
	QN	95
ld6q	Q	47
ld6qd2	Q	95
ld7	Q	47
	QN	47
ld7d2	Q	95
	QN	95
ld8	Q	48
	QN	47
ld8d2	Q	97
	QN	96
oak_ldi2	Q	47
	QN	47
oak_ldi2d2	Q	95
	QN	95
oak_ldi3	Q	47
	QN	47
oak_ldi3d2	Q	95
	QN	95
ls0	Q	44
	QN	44
ls0d2	Q	88
	QN	88
ls1	Q	22
	QN	22
ls1d2	Q	95
	QN	95
mx2	Y	47
mx2d2	Y	95
mx2d4	Y	188
mx2dh	Y	21
mx2i	YN	22
mx2ia	YN	22
mx2id2	YN	95

Cell Name	Output Pin	Maximum Fanouts
mx2id2a	YN	95
mx2id4	YN	192
mx2id4a	YN	191
mx2idh	YN	9
mx2idha	YN	9
mx2ix4	YN0	22
	YN1	22
	YN2	22
	YN3	22
mx2x4	Y0	48
	Y1	48
	Y2	48
	Y3	48
mx3i	YN	46
mx3id2	YN	94
mx3id4	YN	190
mx4	Y	46
mx4d2	Y	92
mx4d4	Y	177
mx8	Y	46
mx8d2	Y	90
mx8d4	Y	170
nd2	Y	45
nd2d2	Y	91
nd2d4	Y	182
nd2dh	Y	20
nd3	Y	30
nd3d2	Y	62
nd3d4	Y	124
nd3dh	Y	14
nd4	Y	23
nd4d2	Y	46
nd4d2b	Y	94
nd4d4	Y	191
nd4dh	Y	10
nd5	Y	47
nd5d2	Y	94
nd5d4	Y	193
nd6	Y	47
nd6d2	Y	95
nd6d4	Y	191
nd8	Y	47
nd8d2	Y	95
nd8d4	Y	191
nid	Y	48
oak_nid10p	Y	2384
nid16	Y	767
nid2	Y	96
oak_nid20p	Y	4731
nid3	Y	142
nid4	Y	192
nid6	Y	283
nid8	Y	378
nidh	Y	20
nit	Y	42
nitd16	Y	758
nitd2	Y	89
nitd4	Y	186
nitd8	Y	373
nitn	Y	41
nitnd16	Y	757
nitnd2	Y	89
nitnd4	Y	186
nitnd8	Y	373
nr2	Y	23

Cell Name	Output Pin	Maximum Fanouts
nr2a	Y	47
nr2d2	Y	47
nr2d2b	Y	96
nr2d4	Y	194
nr2dh	Y	10
nr3	Y	15
nr3a	Y	30
nr3d2	Y	30
nr3d2b	Y	96
nr3d4	Y	194
nr3dh	Y	9
nr4	Y	48
nr4d2	Y	97
nr4d4	Y	195
nr4dh	Y	21
nr5	Y	48
nr5d2	Y	97
nr5d4	Y	194
nr6	Y	48
nr6d2	Y	97
nr6d4	Y	195
nr8	Y	47
nr8d2	Y	95
nr8d4	Y	189
oa21	Y	23
oa211	Y	22
oa2111	Y	21
oa2111d2	Y	94
oa211d2	Y	44
oa211d2b	Y	94
oa211d4	Y	192
oa211dh	Y	10
oa21d2	Y	46
oa21d2b	Y	95
oa21d4	Y	191
oa21dh	Y	10
oa22	Y	21
oa221	Y	18
oa221d2	Y	95
oa221d4	Y	191
oa222	Y	16
oa2222	Y	11
oa2222d2	Y	95
oa2222d4	Y	192
oa222d2	Y	32
oa222d2b	Y	96
oa222d4	Y	192
oa22a	Y	23
oa22d2	Y	42
oa22d2a	Y	47
oa22d2b	Y	96
oa22d4	Y	192
oa22d4a	Y	192
oa22dh	Y	10
oa22dha	Y	10
oa31	Y	14
oa311	Y	14
oa3111	Y	12
oa3111d2	Y	95
oa311d2	Y	94
oa311d4	Y	191
oa31d2	Y	28
oa31d4	Y	191
oa31dh	Y	7
oa32	Y	13

Cell Name	Output Pin	Maximum Fanouts
oa321	Y	12
oa321d2	Y	96
oa321d4	Y	192
oa322	Y	10
oa322d2	Y	95
oa322d4	Y	192
oa32d2	Y	95
oa32d4	Y	191
oa33	Y	11
oa331	Y	11
oa331d2	Y	95
oa331d4	Y	191
oa332	Y	7
oa332d2	Y	95
oa332d4	Y	192
oa33d2	Y	95
oa33d4	Y	193
oa4111	Y	8
oa4111d2	Y	95
or2	Y	47
or2d2	Y	94
or2d4	Y	190
or2dh	Y	21
or3	Y	47
or3d2	Y	97
or3d4	Y	196
or3dh	Y	21
or4	Y	43
or4d2	Y	87
or4d4	Y	191
or4dh	Y	21
or5	Y	43
or5d2	Y	86
or5d4	Y	191
scg1	Y	30
scg1d2	Y	61
scg2	Y	47
scg2d2	Y	94
scg3	Y	30
scg3d2	Y	61
scg4	Y	45
scg4d2	Y	90
scg5	Y	46
scg5d2	Y	93
scg6	Y	47
scg6d2	Y	95
scg7	Y	43
scg7d2	Y	87
scg8	Y	47
scg8d2	Y	95
scg9	Y	47
scg9d2	Y	95
scg10	Y	47
scg10d2	Y	94
scg11	Y	14
scg11d2	Y	30
scg12	Y	23
scg12d2	Y	46
scg13	Y	43
scg13d2	Y	87
scg14	Y	43
scg14d2	Y	87
scg15	Y	30
scg15d2	Y	61
scg16	Y	22
scg16d2	Y	45
scg17	Y	44
scg17d2	Y	90
scg18	Y	30
scg18d2	Y	61
scg19	Y	22
scg19d2	Y	44
scg20	Y	23
scg20d2	Y	47
scg21	Y	14
scg21d2	Y	30
scg22	Y	22
scg22d2	Y	46
scg23	S	47
	CO	46
scg23d2	S	94
	CO	93
xn2	Y	48
xn2d2	Y	95
xn2d4	Y	191
xn3	Y	47
xn3d2	Y	93
xn3d4	Y	176
xo2	Y	47
xo2d2	Y	94
xo2d4	Y	191
xo3	Y	47
xo3d2	Y	94
xo3d4	Y	180

1.8.2 I/O CELLS

The maximum fanouts for I/O cells are as follows.

Table 1-7. Maximum Fanouts of I/O Cells
(t_R/t_F = 0.213ns, one fanout (SL) = 0.006710pF)

Cell Name	Output Pin	Maximum Fanouts
phic	Y	270
phicd	Y	270
phicu	Y	270
phis	Y	270
phisd	Y	270
phisu	Y	270
phit	Y	270
phitd	Y	270
phitu	Y	270
phsosck1	YN	191
phsosck17	YN	191
phsosck2	YN	193
phsosck27	YN	193
phsoscm1	YN	194
phsoscm16	YN	194
phsoscm2	YN	205
phsoscm26	YN	205
phsoscm3	YN	402
phsoscm36	YN	402
pic	Y	131
pic_abb	Y	131
picc_abb	Y	135
picd	Y	131
picen_abb	Y	130
picu	Y	131
pipci	Y	131
pis	Y	130
pisd	Y	130
pisu	Y	130
psosck1	YN	193
psosck2	YN	193
psoscm1	YN	71
psoscm2	YN	251
ptic	Y	270
pticd	Y	270
pticu	Y	270
ptipci	Y	270
ptis	Y	270
ptisd	Y	270
ptisu	Y	270
ptit	Y	270
ptitd	Y	270
ptitu	Y	270

1.8.3 CK CELL MAX FANOUT

STD110 maximum fanout for CK cells

<Condition>

- VDD = 2.5V
- Fanout = 0.00357pF (= input cap for CK pin of FD1)
- Standard Load (SL) = 0.006710pF
- Input slope = 0.213ns
- Max output transition time (mott) =1.5ns
- Maximum frequency $\leq$ 200MHz
- Net length (μm/fanout): branch net length for each fanout except trunk

Table 1-8. Maximum Fanout for CK Cells

Trunk width (μm)	8				In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	5000	10000	5000	10000	
ck2	151	2	32	1	391
ck4	438	264	91	55	781
ck6	711	499	148	104	1172
ck8	966	702	202	146	1561

Table 1-9. Maximum Fanout for NID Cells

Trunk width (μm)	0.44		8		In case that interconnection is not considered
Net length (μm/fanout)	20		200		
Trunk length (μm)	5000	10000	5000	10000	
nid					48
nid2					96
nid3	14				142
nid4	35				192
nid6	69		14		283
nid8	93		28		378
nid16	147		83	46	767
oak_nid10p	200		283	198	2384
oak_nid20p	214		484	307	4731

For high fanout nets including clock net, SEC strongly recommends using clock tree synthesis.

1.9 Package Capability By Lead Count

Package	Lead Inductance	Lead Count							
SOP/SSOP (Small Outline Package)									
		8	16	20	24	28	44	56	70
3.9 x 8.7mm	< 2nH			■					
3.9 x 9.9 mm	< 4nH					■			
4.0 x 5.1mm	< 2nH	■							
4.4 x 6.9 mm	< 3nH		■						
4.4 x 6.9 mm	< 3nH			■					
5.3 x 3.0 mm	< 3nH			■					
5.3 x 7.2 mm	< 3nH			■					
5.3 x 10.2 mm	< 4nH					■			
5.3 x 15.6 mm	< 5nH				■				
5.4 x 14.1 mm	< 5nH			■					
7.5 x 18.4 mm	< 8nH							■	
12.6 x 29.0mm	< 20nH						■		
12.7 x 29.0 mm	< 16nH								■
TSOP/TSSOP (Thin SOP)									
		8	28	32	44	48	54	56	66
4.4 x 3.0mm	< 3nH	■							
4.4 x 9.7 mm	< 3nH		■						
6.1 x 9.7mm	< 3nH		■						
6.1 x 14.0 mm	< 6nH							■	
10.2 x 18.9 mm	< 8nH				■				
10.2 x 21.4 mm	< 7nH			■					
10.2 x 22.6 mm	< 7nH					■	■		■
12.0 x 20.0mm	< 6nH					■			
12.4 x 16.4 mm	< 7nH					■			
PSOP/PSSOP (Power SOP)									
		8	16	20					
3.9 x 9.9 mm	< 3nH		■						
6.1 x 7.64 mm	< 3nH	■							
7.6 x 12.8 mm	< 3nH			■					
11.0 x 15.9 mm	< 6nH		■						

Package	Lead Inductance	Lead Count									
QFP (Quad Flat Package)		44	48	64	80	100	128	160	208	240	256
7 x 7 mm	< 3nH		■								
10 x 10 mm	< 5nH	■	■								
12 x 12 mm	< 5nH				■						
14 x 14 mm	< 6nH			■		■					
14 x 20 mm	< 12nH			■	■	■	■				
24 x 24 mm	< 11nH							■			
28 x 28 mm	< 17nH							■	■		■
32 x 32 mm	< 15nH									■	
TQFP (Thin Quad Flat Package)		32	48	80	100	144	160	176	208		
7 x 7 mm	< 4nH	■	■								
12 x 12 mm	< 5nH			■							
14 x 14 mm	< 5nH				■						
14 x 20 mm	< 10nH				■						
20 x 20 mm	< 9nH					■					
24 x 24 mm	< 11nH						■	■			
28 x 28 mm	< 13nH								■		
PLCC (Plastic Leaded Chip Carrier)		44	84								
16.6 x 16.5mm	<5nH	■									
29.3 x 29.3 mm	< 13nH		■								

Package	Lead Inductance		Lead Count										
SBGA (Super BGA)													
	Lp/g	**Lsig**	256	304	352	432	560	600					
27 x 27 mm	< 3nH	< 7nH	■										
31 x 31 mm	< 3nH	< 8nH		■									
35 x 35 mm	< 3nH	< 8nH			■								
40 x 40 mm	< 3nH	< 9nH				■							
42.5 x 42.5 mm	< 3nH	< 9nH					■						
45 x 45 mm	< 3nH	< 9nH						■					
PBGA (Plastic BGA)													
	Lp/g	**Lsig**	119	121	169	204	208	217	225	249	256	272	300
14 x 22 mm	< 4nH	<9nH	■										
15 x 15 mm	< 4nH	< 13nH		■									
23 x 23 mm	< 4nH	< 18nH			■	■	■	■		■			
27 x 27 mm	< 4nH	< 21nH							■		■	■	■
31 x 31 mm	< 4nH	< 13nH											
35 x 35 mm	< 4nH	< 14nH											
PBGA (Plastic BGA)													
	Lp/g	**Lsig**	304	316	324	329	352	360	385	388	420	456	
14 x 22 mm	< 4nH	<10nH											
15 x 15 mm	< 4nH	< 13nH											
23 x 23 mm	< 4nH	< 18nH											
27 x 27 mm	< 4nH	< 21nH		■	■								
31 x 31 mm	< 4nH	< 13nH	■			■		■	■				
35 x 35 mm	< 4nH	< 14nH					■			■	■	■	

1.10 Power Dissipation

1.10.1 ESTIMATION OF POWER DISSIPATION IN CMOS CIRCUIT

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, the switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and reliability of the device also depend on power dissipation that determines the temperature at which the die operates. To obtain high speed and reliability, designers must estimate power dissipation of the device accurately and determine the appropriate environments including the package and system cooling methods.

This section describes the concepts of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating those in the SEC STD110 library.

1.10.2 STATIC (DC) POWER DISSIPATION

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/ pull-down transistor in the input buffers is about 33μA (at 3.3V) and 25uA (at 2.5V) typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of output and bi-directional buffers is determined by the following formula:

$$P_{DC\_OUTPUT}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) / T$$

$$P_{DC\_BI}\,[mW] = \left(\sum_{k=1}^{n} (V_{OL(k)} \times I_{OL(k)} \times t_{L(k)}) + \sum_{k=1}^{n} ((V_{DD} - V_{OH(k)}) \times I_{OH(k)} \times t_{H(k)}) \right) \times S_{out} / T$$

where,

n = Number of output and bidirectional buffers

T = Total operation time in output mode

t_H = The sum of logic high state time

t_L = The sum of logic low state time

$t_L + t_H = T$ (Supposed that all output and bidirectional buffers have just logic high or low state)

Sout is the output mode ratio of bidirectional buffers (typically 0.5)

1.10.3 DYNAMIC (AC) POWER DISSIPATION

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging a load capacitance, C_L. The energy associated with the switching current for a node capacitance, C_L, is

$$C_L \times V_{DD^2}$$

where V_{DD} is the power supply voltage.

In addition to the power dissipated by the load capacitance, CMOS circuits consume power due to the short-circuit current flowing through a temporary V_{DD}-to-ground path during switching.

The dynamic power dissipation for an entire chip is much more complicated to estimate since it depends on the degree of switching activity of the circuit. SEC has found that the degree of switching activity is 10% on the average and recommends this number to be used in estimating the total dynamic power dissipation.

1.10.4 POWER DISSIPATION IN STD110

This section describes the equations on how to estimate the power dissipation in STD110. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}).

$$P_{TOTAL} = P_{AC} + P_{DC}$$

P_{DC} is negligible in case of CMOS logic.

The dynamic power dissipation is caused by three components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), bidirectional buffers (P_{AC_BI}), and internal cells ($P_{AC\_INTERNAL}$).

$$P_{AC} = P_{AC\_INPUT} + P_{AC\_OUTPUT} + P_{AC\_BI} + P_{AC\_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

$$P_{AC\_INPUT}\,[mW] = 2.5\times \sum_{j}^{N\_2.5V\_input}\left(I_{j\_eq\_p}\times\frac{F_j}{100}\times S_j\right) + 3.3\times \sum_{k}^{N\_3.3V\_input}\left(I_{k\_eq\_p}\times\frac{F_k}{100}\times S_k\right) + 6.25\times \sum_{i}^{N\_total\_input}(0.001\times S_i\times F_i\times C_{i\_inload})$$

$$P_{AC\_OUTPUT}\,[mW] = 2.5\times \sum_{i}^{N\_2.5V\_output}\left(I_{i\_eq\_p}\times\frac{F_i}{100}\times S_i\right) + 3.3\times \sum_{j}^{N\_3.3V\_output}\left(I_{j\_eq\_p}\times\frac{F_j}{100}\times S_j\right) + 6.25\times \sum_{i}^{N\_2.5V\_output}(0.001\times S_i\times F_i\times C_{i\_outload}) + 10.89\times \sum_{j}^{N\_3.3V\_output}(0.001\times S_j\times F_j\times C_{j\_outload})$$

$$P_{AC\_BI}\,[mW] = P_{AC\_BI\_INPUT}\times(1-S_{out}) + P_{AC\_BI\_OUTPUT}\times S_{out}$$

$$P_{AC\_BI\_INPUT}\,[mW] = 2.5\times \sum_{j}^{N\_2.5V\_bi}\left(I_{j\_eq\_p}\times\frac{F_j}{100}\times S_j\right) + 3.3\times \sum_{k}^{N\_3.3V\_bi}\left(I_{k\_eq\_p}\times\frac{F_k}{100}\times S_k\right) + 6.25\times \sum_{i}^{N\_total\_bi}(0.001\times S_i\times F_i\times C_{i\_inload})$$

$$P_{AC\_BI\_OUTPUT}\,[mW] = 2.5\times \sum_{i}^{N\_2.5V\_bi}\left(I_{i\_eq\_p}\times\frac{F_i}{100}\times S_i\right) + 3.3\times \sum_{j}^{N\_3.3V\_bi}\left(I_{j\_eq\_p}\times\frac{F_j}{100}\times S_j\right) + 6.25\times \sum_{i}^{N\_2.5V\_bi}(0.001\times S_i\times F_i\times C_{i\_outload}) + 10.89\times \sum_{j}^{N\_3.3V\_bi}(0.001\times S_i\times F_i\times C_{i\_outload})$$

$$P_{AC\_INTERNAL}\,[mW] = 0.001\times(0.2317\times S + 0.0167)\times G\times F + \sum_{j}^{N\_macro}(0.001\times P_i\times F_i)$$

where

N_2.5V_input is the number of 2.5V interface input buffers used
N_3.3V input is the number of 3.3V interface input buffers used,
N_total_input = N_2.5V_input + N_3.3V input
N_2.5V_output is the number of 2.5V interface output buffers used,
N_3.3V_output is the number of 3.3V interface output buffers used,
N_2.5V_bi is the number of 2.5V interface bidirectional buffers used,
N_3.3V_bi is the number of 3.3V interface bidirectional buffer used,
N_macro is the number of macro cells used,
G is the size of the design in gate count,
F is the operating frequency in MHz,
S is the estimated degree of switching activity (typically 0.1 for internal and 0.5 for I/O),
Sout is the output mode ratio of bidirectional buffers (typically 0.5),
C is the load capacitance in pF.
P is the characterized power for the i-th hard macro block (μW/MHz)

1.10.5 TEMPERATURE AND POWER DISSIPATION

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{TOTAL}$$

where

θ_{JA} is the thermal impedance,
T_J is the junction temperature of the device,
T_A is the ambient temperature.

Thermal impedances of the SEC packages are given in the following table. The junction temperature, obtained by multiplying P_{TOTAL} by the appropriate θ_{JA} and adding T_A, determines the derating factor for the propagation delays and also indicates the reliability measures. Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-10. Thermal Impedances of SEC Plastic Packages

	SOP/TSOP								
Pin Number	**20**	**24**	**28**	**32**	**44**	**50**	**54**	**62**	**66**
θ_{JA}[°C/W]	63	58	41-44	46-56	44-71	39-59	34-56	27-33	34-46

	QFP									
Pin Number	**44**	**48**	**80**	**100**	**120**	**128**	**160**	**208**	**240**	**256**
θ_{JA}[°C/W]	51-62	43-56	43-74	27-61	33-47	43-51	29-51	22-43	28-47	29-42

	TQFP/LQFP							
Pin Number	**32**	**64**	**100**	**144**	**160**	**176**	**208**	**256**
θ_{JA}[°C/W]	68-70	47	37-70	38	35-62	31-34	37-56	30-42

	PBGA			
Pin Number	**272**	**388**	**356 (TEPBGA)**	**452 (TEPBGA)**
θ_{JA}[°C/W]	19-22	16-19	16	14

	SBGA				
Pin Number	**256**	**304**	**352**	**432**	**600**
θ_{JA}[°C/W]	14.1	13.1	11.7	10.2	8.3

1.11 V_{DD}/V_{SS} Rules And Guidelines

There are three kinds of VDD and VSS in STD110, providing power to internal and I/O area.

- Core logic
  – VDD2I, VSS2I
- Pre-driver (I/O area)
  – VDD2P, VDD3P, VSS2P, VSS3P
- Output-drive (I/O area)
  – VDD2O, VDD3O, VSS2O, VSS3O

The number of VDD and VSS pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency

1.11.1 BASIC PLACEMENT GUIDELINES

The purpose of these guidelines is to minimize IR drop and noise for reliable device operations.

- Core logic and pre-driver V_{DD}/V_{SS} pads should be evenly distributed on all sides of the chip.
- If you have core block demanding high power (compiled memory, analog), extra power pads should be placed on that side.
- Power pads for SSO group should be evenly distributed in the SSO group.
- Do not place the quiet signal (analog, reference) or analog power (VDDA/VSSA) or bi-directional buffer next to a SSO group.
- The opposite types of power pads (V_{DD}/V_{SS}) should be placed as close as possible.
- If it is possible, do not place power pads (V_{DD}/V_{SS}) at the corner of the chip.

1.11.2 VDD2I/VSS2I ALLOCATION GUIDELINES

The purpose of these guidelines is to ensure that the minimum number of core logic power pad pairs meeting the electromigration current limit are used. The number of VDD2I/VSS2I pads required for a specific design is determined by the function of the operating frequency of a chip.

- VDD2I bus width and the number of pads are equal to those of VSS2I
- VDD2I/VSS2I buses and pads should be distributed evenly in the core and on each side of the chip.
- The total number of core logic VDD2I pads is equal to that of VSS2I pads.

The number of VDD2I/VSS2I pad pairs required for a design can be calculated from the following expression:
The number of VDD2I/VSS2I pad pairs =

$$\left\| \left[0.001 \times (0.0927 \times S + 0.0067) \times G \times F + \sum_{i}^{N\_macro} (Pi \times Fi) \right] / I_{em} \right\| round-up$$

where,

G = The core (excluding hard macro blocks) size in the gate counts
S = The switching ratio (typically = 0.1)
F = Operating frequency (MHz)
Pi = Characterized current for the i-th hard macro block (mA/MHz)
Fi = Operating frequency for the i-th hard macro block (MHz)
I_{em} = Current limit per VDD/VSS pad pairs based on ElectroMigration rule (80mA)

For reliable device operation and minimize IR voltage drop, minimum number of VDD2I/VSS2I power pad pairs is 4.

Extra power may be needed for the demanding high power macro blocks (SRAM, analog block...).

1.11.3 VDD2P/VSS2P (VDD3P/VSS3P) ALLOCATION GUIDELINES.

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.
The number of VDD2P/VSS2P (VDD3P/VSS3P) pads required for a design can be calculated from the following expression:

$$Number\_ of\_VDD2P/VSS2P(VDD3P/VSS3P)\ pairs = \left\| \frac{I_{eq\_p}}{I_{em}} \right\| round-up$$

In above expression,
I_{eq_p} = ∑(Average current of input/output buffers and bi-direction pre-drivers at maximum operational I/O frequency) [mA] (Refer Table 1-11)

$$I_{eq\_p} = \sum_{i}^{N\_input} \left(I_{eq\_p\_in} \times \frac{F_i}{100} \right) + \sum_{j}^{N\_output} \left(I_{j\_eq\_p\_out} \times \frac{F_j}{100} \right) + \sum_{k}^{N\_bi} \left[\left(I_{k\_eq\_p\_in} \times \frac{F_k}{100} \right) (1 - S_{out}) + \left(I_{k\_eq\_p\_out} \times \frac{F_k}{100} \right) \times S_{out} \right]$$

where

N_input is the number of input buffers used,
N_output is the number of output buffers used,
N_bi is the number of bi-directional buffers used,
F is the operating frequency in MHz,
S_{out} is the output mode ratio of bi-directional buffers (typically 0.5),
I_{em} = Current limit per VDD/VSS pad pairs based on electromigration rule. (80mA)

Table 1-11. 2.5V Interface

Input Buffer Type		**CMOS**			**CMOS Schmitt**		
Ieq_p (mA)		0.35			0.36		
Output Pre-Driver Type		**Driver**			**Tristate**		
		B1–4	**B6–8**	**B10–12**	**T1–4**	**T6–8**	**T10–12**
Ieq_p (mA)	Normal	0.14	0.27	0.41	0.24	0.36	0.53
	Slew rate	0.14	0.25	0.35	0.25	0.35	0.45

Table 1-12. 3.3V Interface

Input Buffer Type			CMOS		TTL	Schmitt Trigger		
Ieq_p (mA)	Normal		0.52		0.54	0.54		
	Tolerant		0.60		0.60	0.51		
Output Pre-driver Type			CMOS Driver			Tristate		
			B1–4	B6–8	B10–12	T1–4	T6–8	T10–12
Ieq_p (mA)	Normal	Normal	0.25	0.46	0.55	0.34	0.51	0.60
		Slew rate	0.28	0.37	0.46	0.36	0.45	0.55
	Tolerant		-	-	-	(T1,2,3) 0.50	-	-

For reliable device operation and minimum IR voltage drop, at least 4 pairs of VDD2P/VSS2P (VDD3P/VSS3P) power pads are needed.

1.11.4 VDD2O/VSS2O (VDD3O/VSS3O) ALLOCATION GUIDE

SSO (Simultaneous Switching Output) current induced in power and ground inductance can cause system failure because of voltage fluctuations. For the calculation of output drive power pad numbers, we consider the SSO noise as well as the current limit based on electromigration. We may define the SSO as outputs switching simultaneously in 1ns windows, such as bus type buffers.

NOTE: In case of heavy load, high frequency and low package inductance, the number of power pads for SSO block could be determined by electromigration rule rather than limit of SSO noise. So the number of power pads for SSO block should be determined as the worse one of the power pad number under the limit of SSO noise and that under the limit of electromigration rule.

1) Number of power pads for SSO block

- Number of power pads for SSO block under the limit of SSO noise

- Calculating the number of power pad for each SSO group from the following expressions:

$$NVDDO_{each\_SSO} = \frac{number\_of\_SSO}{NBvdd} \times L_{pg} \times \frac{1}{D_{SSO\_mode}}$$

$$NVSSO_{each\_SSO} = \frac{number\_of\_SSO}{NBvss} \times L_{pg} \times \frac{1}{D_{SSO\_mode}}$$

In above formula,

$NVDDO_{each\_sso}$ = Number of VDD2O (VDD3O) pad required for each SSO group

$NVSSO_{each\_sso}$ = Number of VSS2O (VSS3O) pad required for each SSO group

NBvdd =Number of buffers per VDD2O (VDD3O) power pad with 1nH lead inductance

NBvss = Number of buffers per VSS2O (VSS3O) ground pas with 1nH lead inductance

L_{pg} = Package lead frame inductance
(refer to 1.9 package capability by lead count)

$D_{sso\_mode} = D_{L\_mode} \times D_{P\_mode} \times D_{V\_mode} \times D_{T\_mode} \times D_{C\_mode}$ (Refer to Table 1-13. and Table 1-14.)

D_{L_mode} = Lead inductance derating factor
D_{P_mode} = Process derating factor
D_{V_mode} = Voltage derating factor
D_{T_mode} = Temperature derating factor
D_{C_mode} = Cload derating factor (*mode is either vdd or vss.)

Table 1-13. Derating Equation (external 2.5V interface)

Item	Mode	Equation	Range
Package Lead	D_{L_vdd}	0.0417 x Lpg + 0.9375 0.0417 x Lpg + 0.9375	3nH ≤ Lpg ≤ 10nH 10nH ≤ Lpg ≤ 15nH
	D_{L_vss}	0.0417 x Lpg + 0.9375 0.0417 x Lpg + 0.9375	3nH ≤ Lpg ≤ 10nH 10nH < Lpg ≤ 15nH
Process	D_{P_vdd}	1.0000 1.2549 1.7255	best typical worst
	D_{P_vss}	1.0000 1.2549 1.7451	best typical worst
Voltage	D_{V_vdd}	– 0.8824 x voltage + 3.3235 – 0.5882 x voltage + 2.5882	2.3 ≤ voltage ≤ 2.5 2.5 < voltage ≤ 2.7
	D_{V_vss}	– 0.8824 x voltage + 3.3235 – 0.5882 x voltage + 2.5882	2.3 ≤ voltage ≤ 2.5 2.5 < voltage ≤ 2.7
Temperature	D_{T_vdd}	0.0024 x temperature + 1.0000 0.0032 x temperature + 0.9786	-40 ≤ temperature ≤ 25 25 < temperature ≤ 125
	D_{T_vss}	0.0031 x temperature + 1.0000 0.0029 x temperature + 1.0071	-40 ≤ temperature ≤ 25 25 < temperature ≤ 125
Cload	D_{C_vdd}	0.0347 x Cload + 0.6525 0.0286 x Cload + 0.8369	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF
	D_{C_vss}	0.0354 x Cload + 0.6456 0.0285 x Cload + 0.8544	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF

Table 1-14. Derating Equation (external 3.3V interface)

Item	Mode	Equation	Range
Package Lead	D_{L_vdd}	0.0462 x Lpg + 1.1538 0.0231 x Lpg + 1.3846	3nH ≤ Lpg ≤ 10nH 10nH ≤ Lpg ≤ 15nH
	D_{L_vss}	0.0469 x Lpg + 0.7813 0.0313 x Lpg + 0.9375	3nH ≤ Lpg ≤ 10nH 10nH < Lpg ≤ 15nH
Process	D_{P_vdd}	1.0000 1.2537 2.2985	best typical worst
	D_{P_vss}	1.0000 1.1563 1.4063	best typical worst
Voltage	D_{V_vdd}	– 1.2936 x voltage + 5.4328 – 0.4478 x voltage + 2.6119	3.0 ≤ voltage ≤ 3.3 3.3 < voltage ≤ 3.6
	D_{V_vss}	– 0.4166 x voltage + 2.5000 – 0.4166 x voltage + 2.5000	3.0 ≤ voltage ≤ 3.3 3.3 < voltage ≤ 3.6
Temperature	D_{T_vdd}	0.0036 x temperature + 1.0000 0.0041 x temperature + 0.9878	-40 ≤ temperature ≤ 25 25 < temperature ≤ 125
	D_{T_vss}	0.0038 x temperature + 1.0000 0.0028 x temperature + 1.0227	-40 ≤ temperature ≤ 25 25 < temperature ≤ 125
Cload	D_{C_vdd}	0.0338 x Cload + 0.6618 0.0554 x Cload + 0.0146	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF
	D_{C_vss}	0.0444 x Cload + 0.5556 0.0370 x Cload + 0.7778	10pF ≤ Cload ≤ 30pF 30pF < Cload ≤ 50pF

Table 1-15. NBvdd/NBvss Parameter (Process = best, Volt =2.7V/3.6V Temp. = 0˚C, Llead = 1nH)

Buffer Type	Voltage Type	Normal		Slew-Rate Medium (sm)		Slew-Rate High (sh)	
		NBvdd	NBvss	NBvdd	NBvss	NBvdd	NBvss
pob1 (pot1)	2.5V Interface	176	178	–	–	–	–
pob2 (pot2)		140	142	–	–	–	–
pob4 (pot4)		102	102	160	160	–	–
pob6 (pot6)		84	84	142	142	–	–
pob8 (pot8)		72	72	116	116	–	–
pob12 (pot12)		60	60	96	96	236	236
phob1 (phot1)	3.3V Interface	382	166	–	–	–	–
phob2 (phot2)		276	104	–	–	–	–
phob4 (phot4)		134	64	168	104	–	–
phob6 (phot6)		108	44	132	90	–	–
phob8 (phot8)		98	38	118	86	–	–
phob12 (phot12)		86	32	92	62	130	124
ptot1	5V Tolerant	434	376	–			
ptot2		272	180				
ptot3		203	116				

NOTE: pob1 means 1mA output driver cell, and pob12 means 12mA output driver cell.

- Calculating the number of required power pad for total SSO from the following expression:

  $NVDDO1sso = \sum NVDDOeach\_sso$
  $NVSSO1sso = \sum NVSSOeach\_sso$

  In the above formula,

  NVDDOsso = Number of VDD2O (VDD3O) pad per total SSO buffers
  NVSSOsso = Number of VSS2O (VSS3O) pad per total SSO buffers

- Number of power pads for SSO block under the limit of electromigration rule

- Calculating the following expression:

$$NVDDO2_{SSO}/NVSSO2_{SSO} = \frac{I_{eq\_o}}{I_{em}}$$

$$I_{eq\_o} = \sum_{i}^{N\_SSO\_output} (0.001 \times C_{i\_outload} \times V_i \times F_i \times S_i) + \sum_{j}^{N\_SSO\_bi} (0.001 \times C_{j\_outload} \times V_j \times F_j \times S_j \times S_{j\_out})$$

where

N_SSO_output is the number of simultaneous switching output buffers used,
N_SSO_bi is the number of simultaneous switching bi-directional buffers used,
$C_{outload}$ = Output load capacitance [pF]
V = Operating voltage [V]
F = Maximum I/O operating frequency [MHz]
S = Switching ratio (typically 0.5)
S_{out} = Output mode ratio of bidirectional buffers (typically 0.5)
I_{em} = Current limit per VDD/VSS pad paris based on electromigration rule. (80mA)

2) Number of power pads for non-SSO block

- Calculating the following expression:

$$NVDDO_{non\_SSO}/NVSSO_{non\_SSO} = \frac{I_{eq\_o}}{I_{em}}$$

$$I_{eq\_o} = \sum_{i}^{N\_non\_SSO\_output} (0.001 \times C_{i\_outload} \times V_i \times F_i \times S_i) + \sum_{j}^{N\_non\_SSO\_bi} (0.001 \times C_{j\_outload} \times V_j \times F_j \times S_j \times S_{j\_out})$$

where

N_non_SSO_output is the number of non-simultaneous switching output buffers used,
N_non_SSO_bi is the number of non-simultaneous switching bi-directional buffers used,
$C_{outload}$ = Output load capacitance [pF]
V = Operating voltage [V]
F = Maximum I/O operating frequency [MHz]
S = Switching ratio (typically 0.5)
S_{out} = Output mode ratio of bidirectional buffers (typically 0.5)
I_{em} = Current limit per VDD/VSS pad paris based on electromigration rule. (80mA)

3) Total number of power pads for VDD2O/VSS2O (VDD3O/VSS3O)

- Calculating the following expressions:

$$\text{Number of VDD2O (VDD3O)} = \left\| \max(NVDDO1_{SSO}, NVDDO2_{SSO}) + NVDDO_{non\_SSO} \right\| \text{ round-up}$$

$$\text{Number of VSS2O (VSS3O)} = \left\| \max(NVSSO1_{SSO}, NVSSO2_{SSO}) + NVSSO_{non\_SSO} \right\| \text{ round-up}$$

When open drain type buffers are used, you can consider using VSS2O (VSS3O) pads since they have current sink only.

1.12 Crystal Oscillator Consideration

1.12.1 OVERVIEW

STD110 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that SEC cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, any more than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30 ohms for some given frequency. Then your crystal supplier tells you the 30 ohm crystals are going to cost twice as much as 50 ohm crystals. Fearing that SEC will not “guarantee operation” with 50 ohm crystals, you order the expensive ones.

In fact, SEC guarantees only what is embodied within an SEC product. Besides, there is no reason why 50 ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50 ohm crystals or 30 ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

1.12.2 OSCILLATOR DESIGN CONSIDERATIONS

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

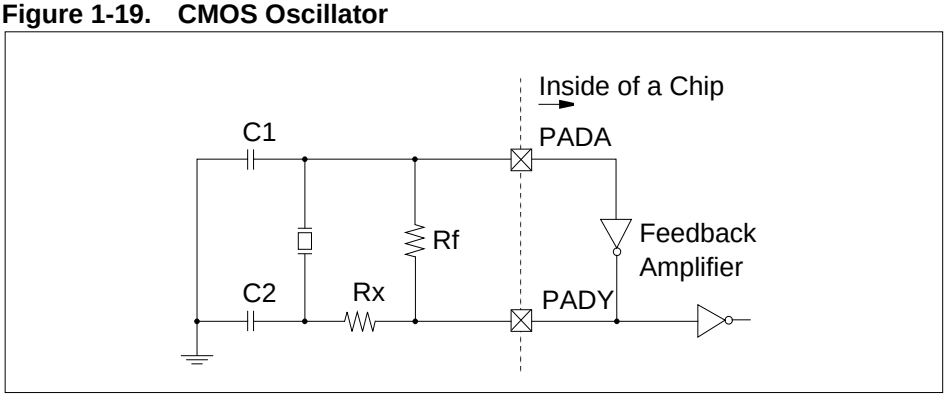
The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

1.12.2.1 On-Chip Oscillator

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

Figure 1-19. CMOS Oscillator



1.12.2.2 Crystal Specifications

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can't be compensated for by appropriate selection of the capacitance, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking "ppm" tolerances with radio engineers and simply won't take your order until you've filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don't pay for 0.003% crystals if your actual frequency tolerance is 1%.

1.12.2.3 Oscillation Frequency

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7 pF each.

Internal phase deviations capacitance of 25 to 30 pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

1.12.2.4 C1 / C2 Selection

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 15pF. (But they don’t have to be either.)

Increasing the value of these capacitances above some 40 or 50 pF improves frequency stability. It also tends to increase the start-up time. These is a maximum value (several hundred pH, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won’t start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 15 and 50pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

1.12.2.5 Rf / Rx Selection

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which testabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-19.

At higher frequencies a 20 or 30 pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.

1.12.2.6 Pin Capacitance Rf / Rx Selection

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF.

The PADY-to-ground cap. is not entirely a “pin capacitance”, but more like an “equivalent output capacitance” of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

1.12.2.7 Placement of Components

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins.

If possible, use dedicated V_{SS} and V_{DD} pin for only crystal feedback amplifier.

1.12.3 TROUBLESHOOTING OSCILLATOR PROBLEMS

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quit” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

PADA through the resonator to PADY;
PADA through C1 to the V_{SS} pin;
PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the V_{SS} pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.